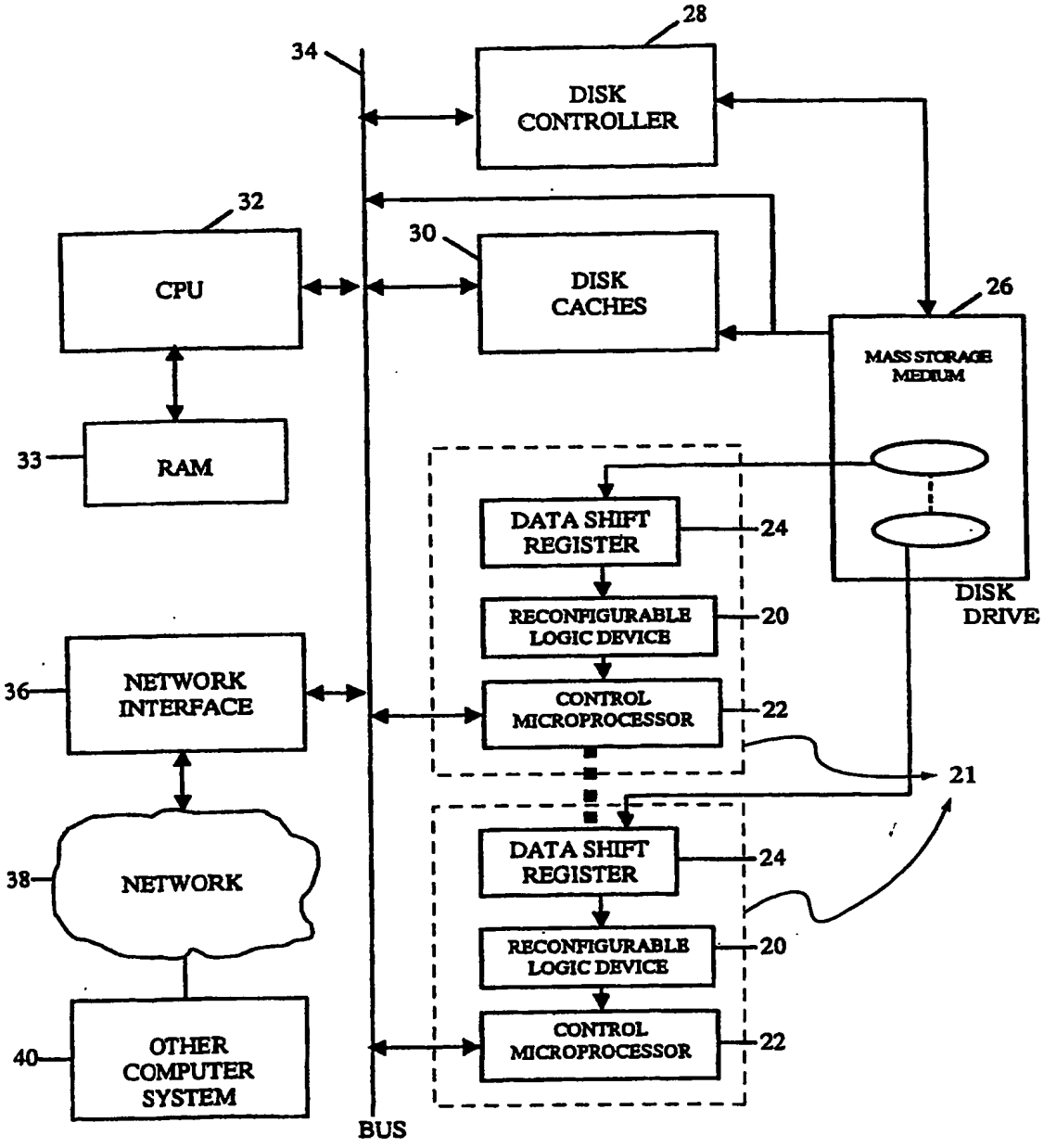


Figure 1

BEST AVAILABLE COPY

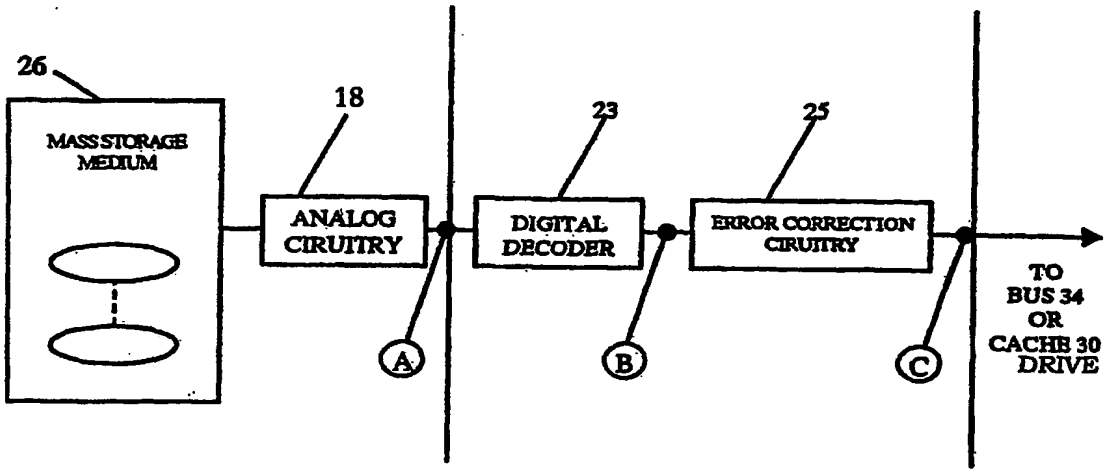

26
MASS STORAGE MEDIUM
18
ANALOG CIRUITRY
23
DIGITAL DECODER
25
ERROR CORRECTION CIRUITRY
TO BUS 34 OR CACHE 30 DRIVE
A
B
C

Figure 2

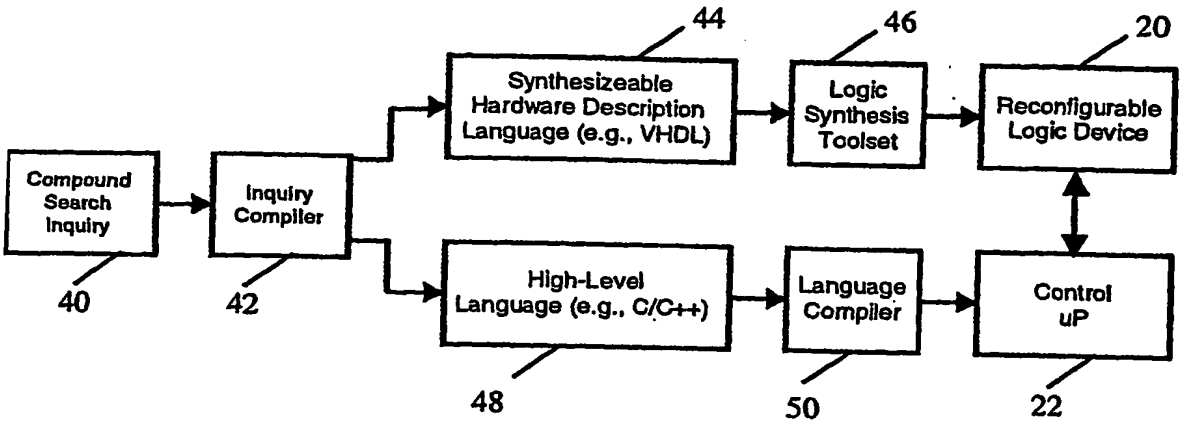

Compound Search Inquiry
Inquiry Compiler
Synthesizeable Hardware Description Language (e.g., VHDL)
Logic Synthesis Toolset
Reconfigurable Logic Device
High-Level Language (e.g., C/C++)
Language Compiler
Control uP
40
42
44
46
20
48
50
22

Figure 3

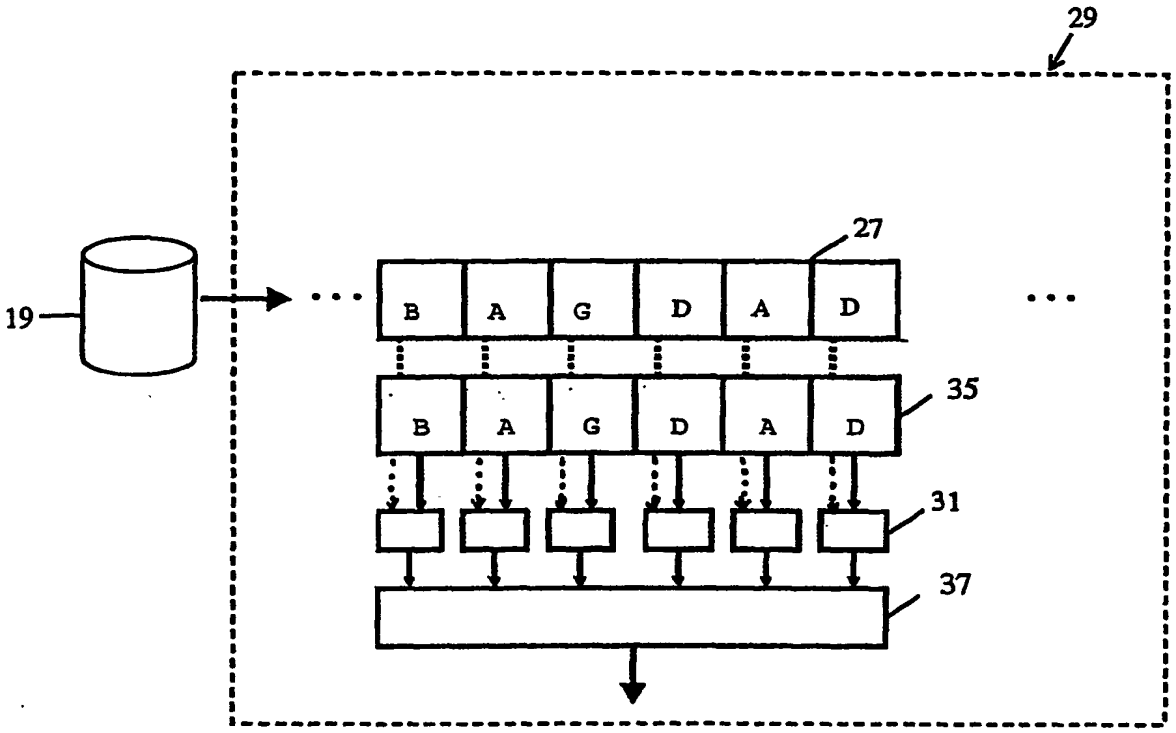


Figure 4

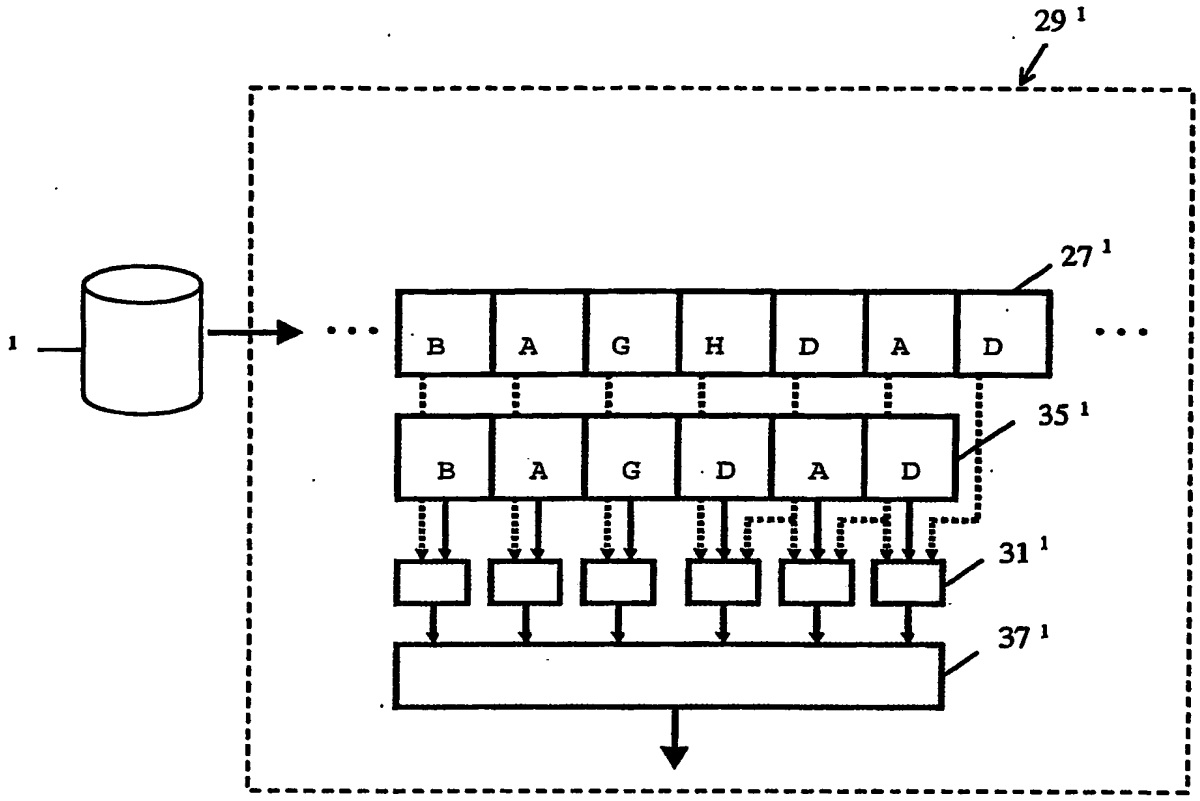


Figure 5

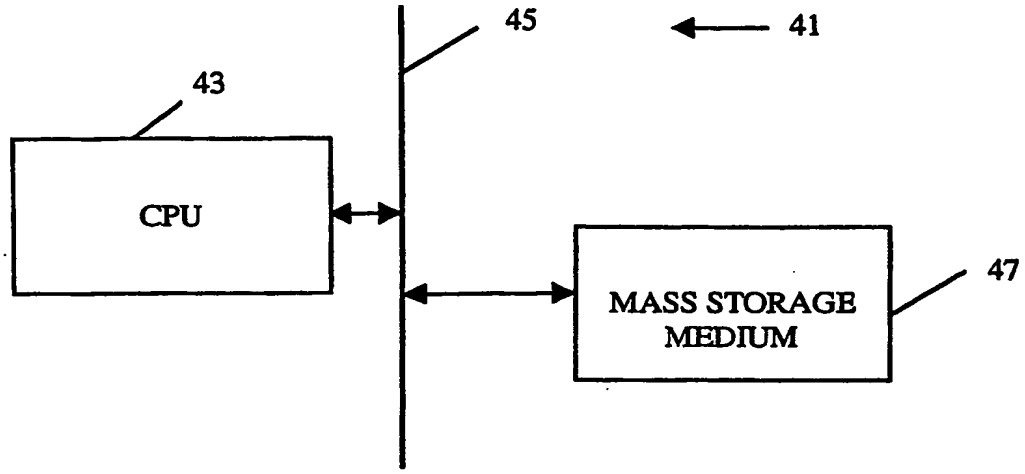


Figure 6

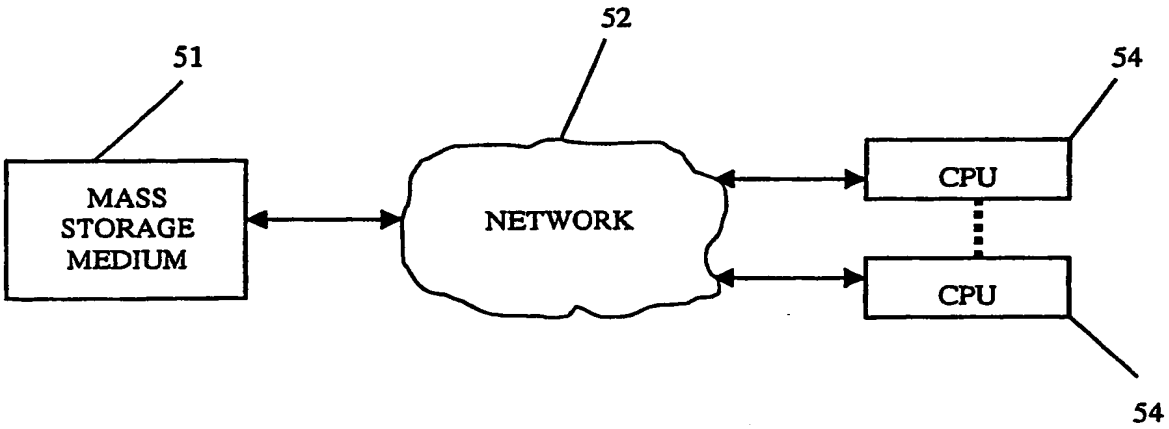


Figure 7

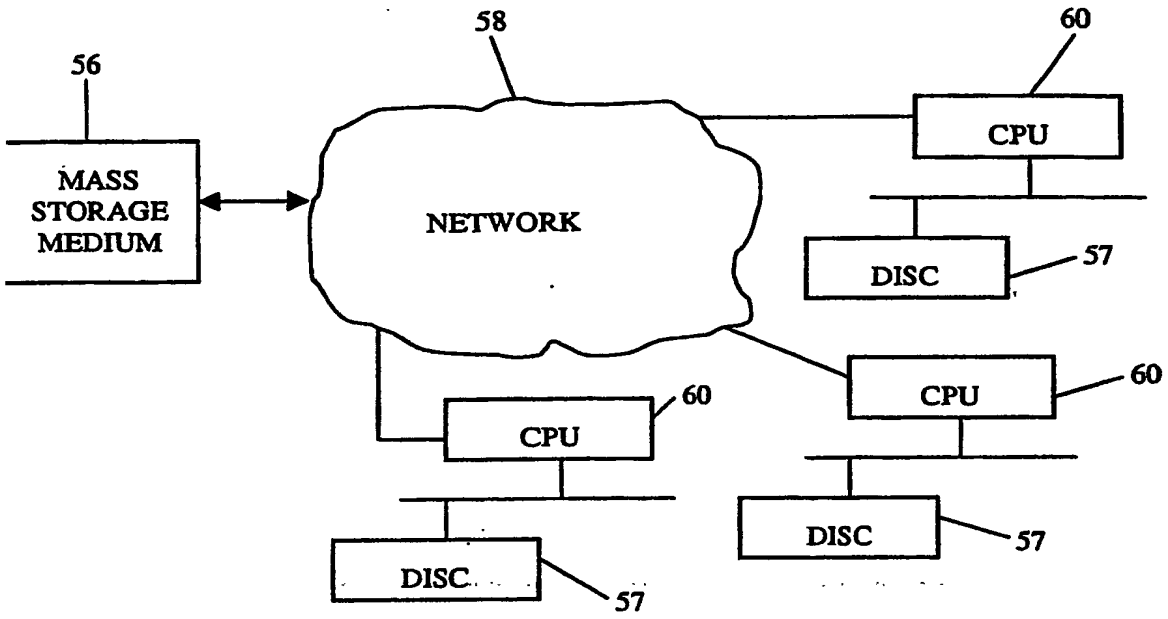

58
60
56
CPU
MASS STORAGE MEDIUM
NETWORK
DISC
57
CPU
60
60
CPU
DISC
57
DISC
57

Figure 8

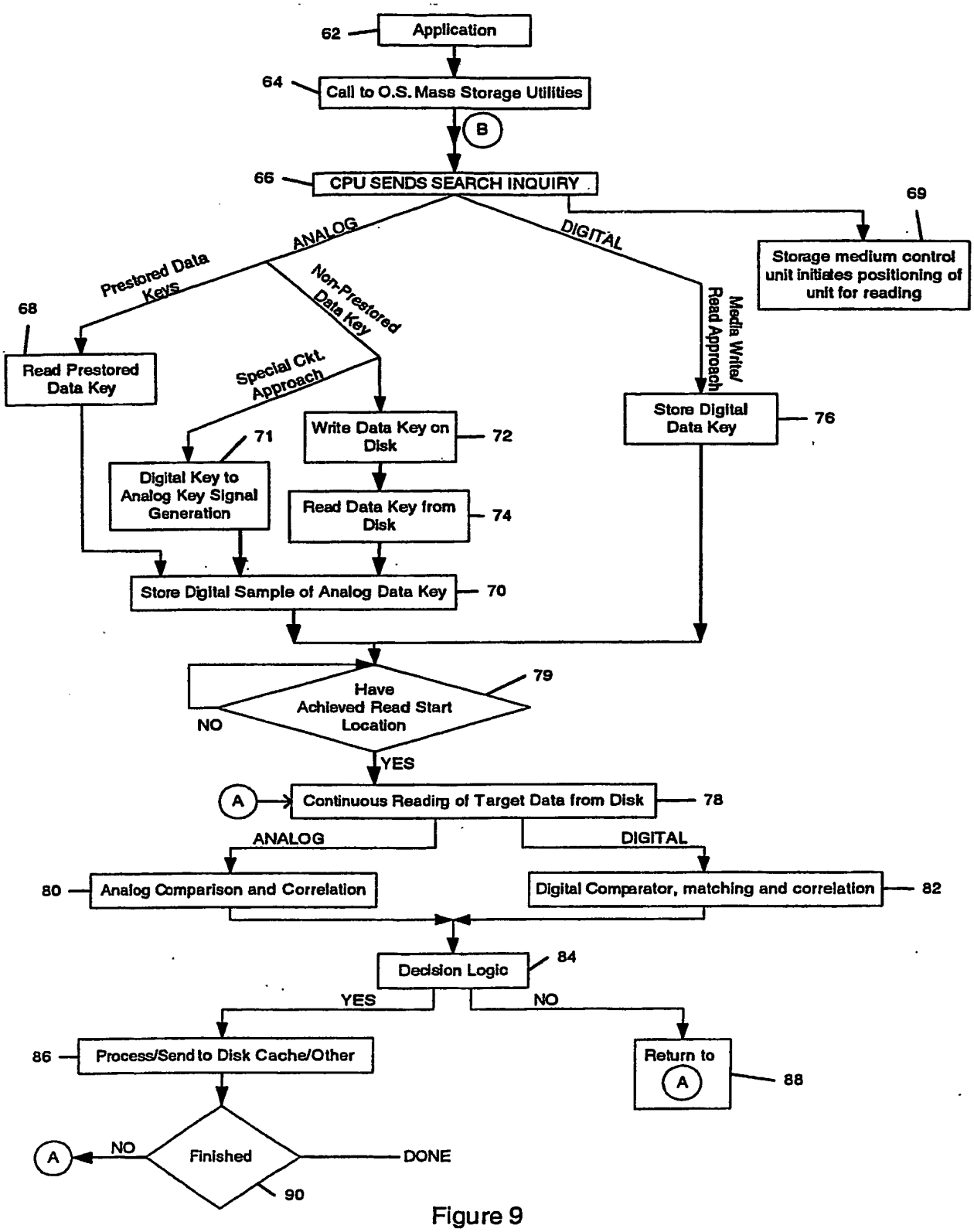

62
Application
64
Call to O.S. Mass Storage Utilities
B
66
CPU SENDS SEARCH INQUIRY
69
Storage medium control unit initiates positioning of unit for reading
ANALOG
DIGITAL
Prestored Data Keys
Non-Prestored Data Key
Media Write/ Read Approach
68
Read Prestored Data Key
Special Ckt. Approach
71
Digital Key to Analog Key Signal Generation
Write Data Key on Disk
72
Read Data Key from Disk
74
Store Digital Data Key
76
Store Digital Sample of Analog Data Key
70
79
Have Achieved Read Start Location
NO
YES
A
Continuous Reading of Target Data from Disk
78
ANALOG
DIGITAL
80
Analog Comparison and Correlation
Digital Comparator, matching and correlation
82
Decision Logic
84
YES
NO
86
Process/Send to Disk Cache/Other
Return to A
88
A
NO
Finished
DONE
90

Figure 9

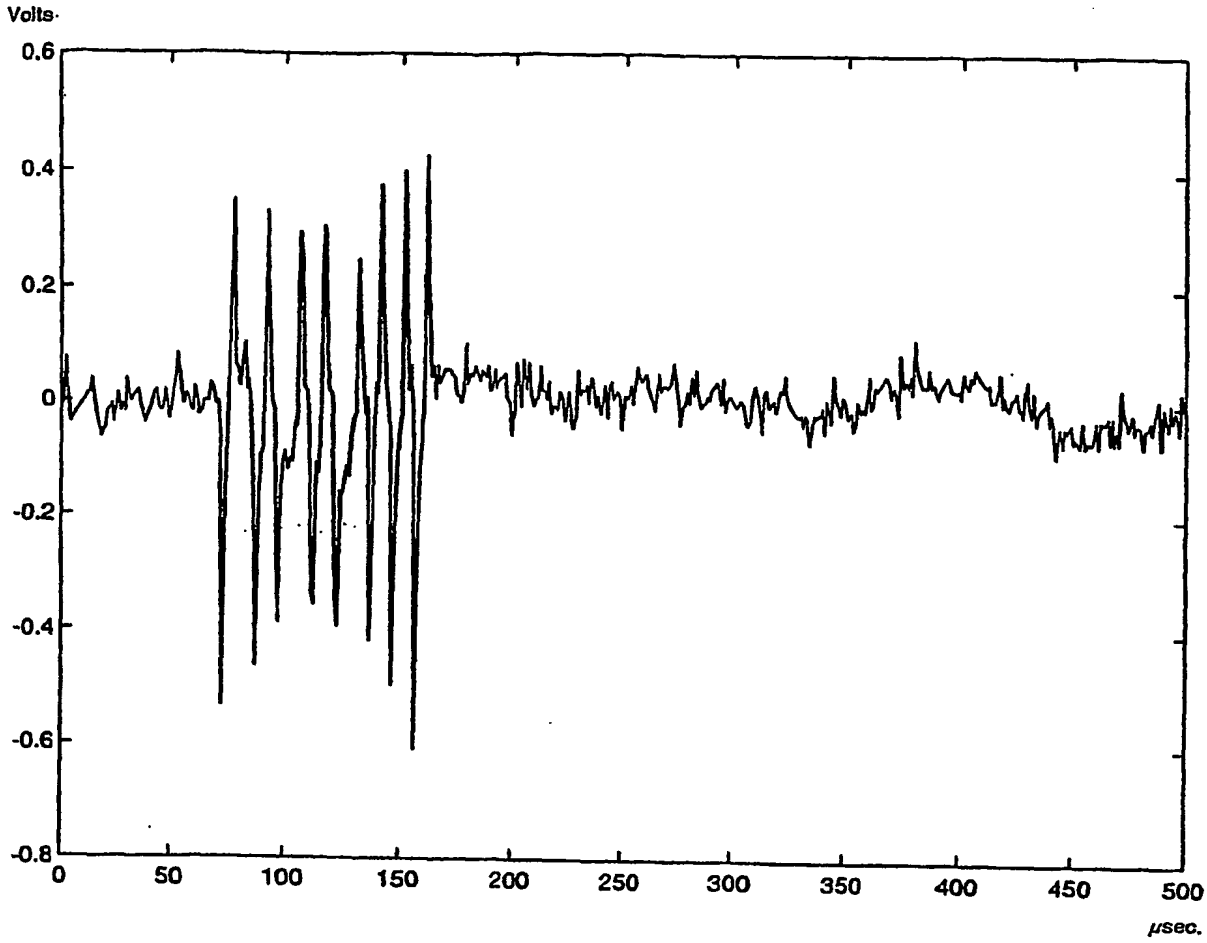

Volts
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
50
100
150
200
250
300
350
400
450
500
μsec.

Figure 10

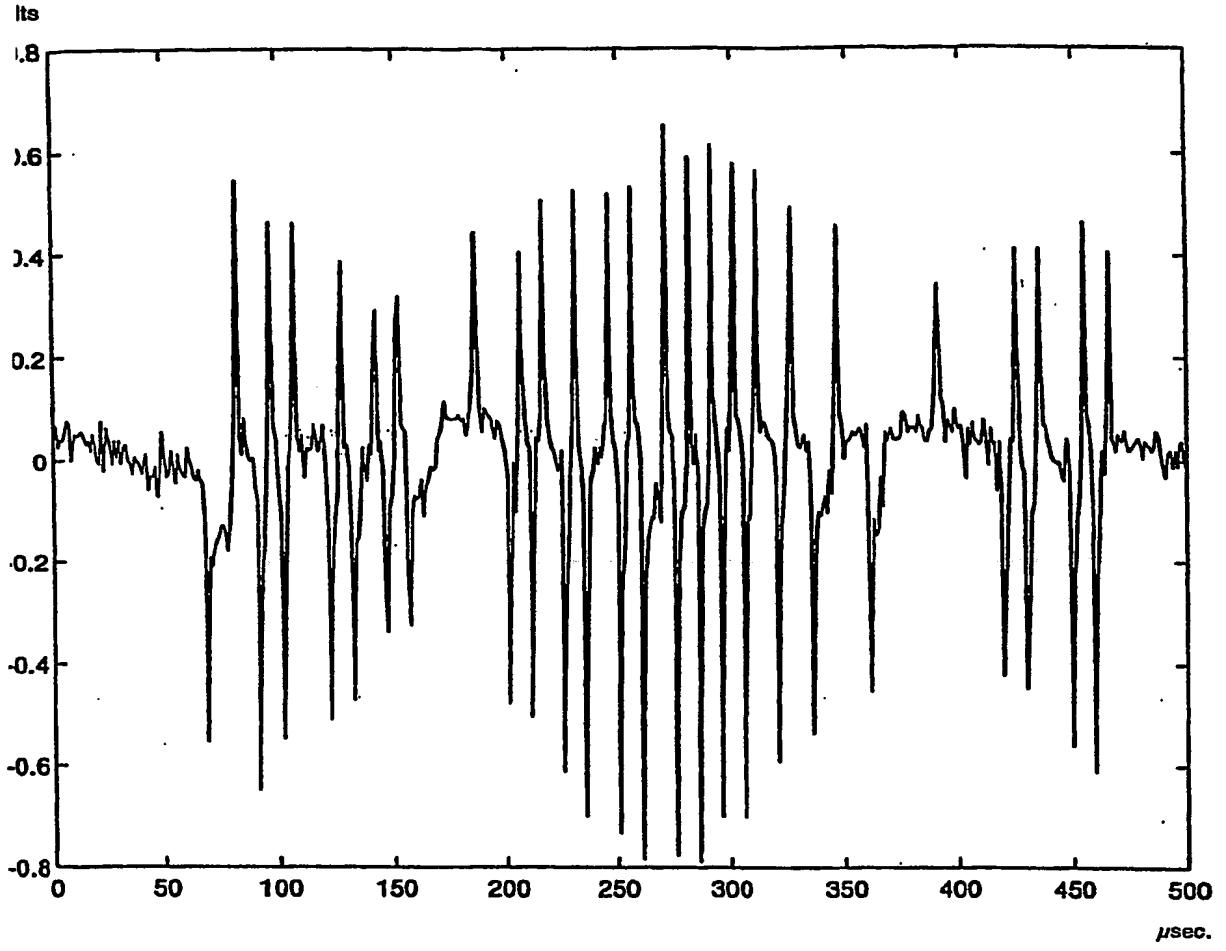

lts
.8
.6
.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
50
100
150
200
250
300
350
400
450
500
μsec.

Figure 11

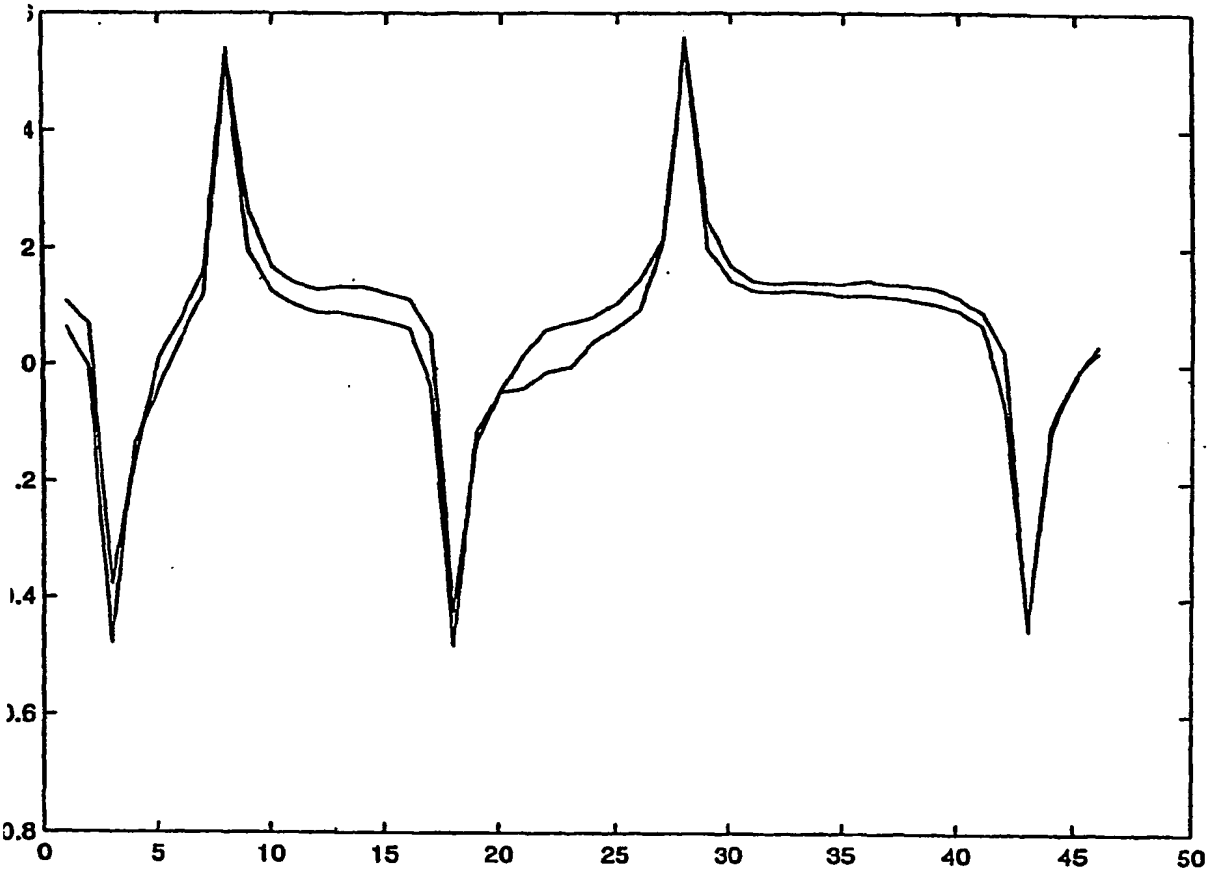


Figure 12

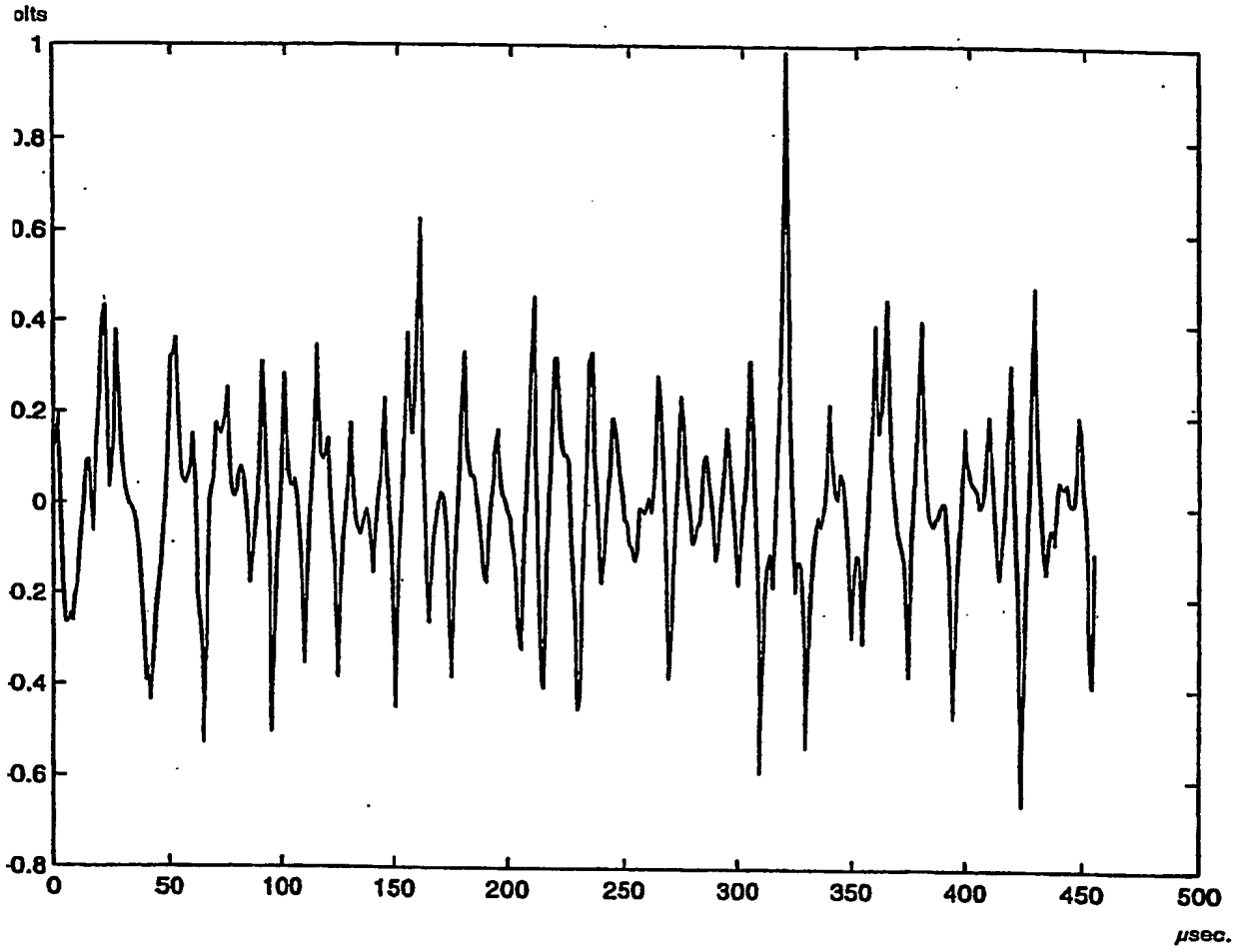

olts
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
50
100
150
200
250
300
350
400
450
500
μsec.

Figure 13

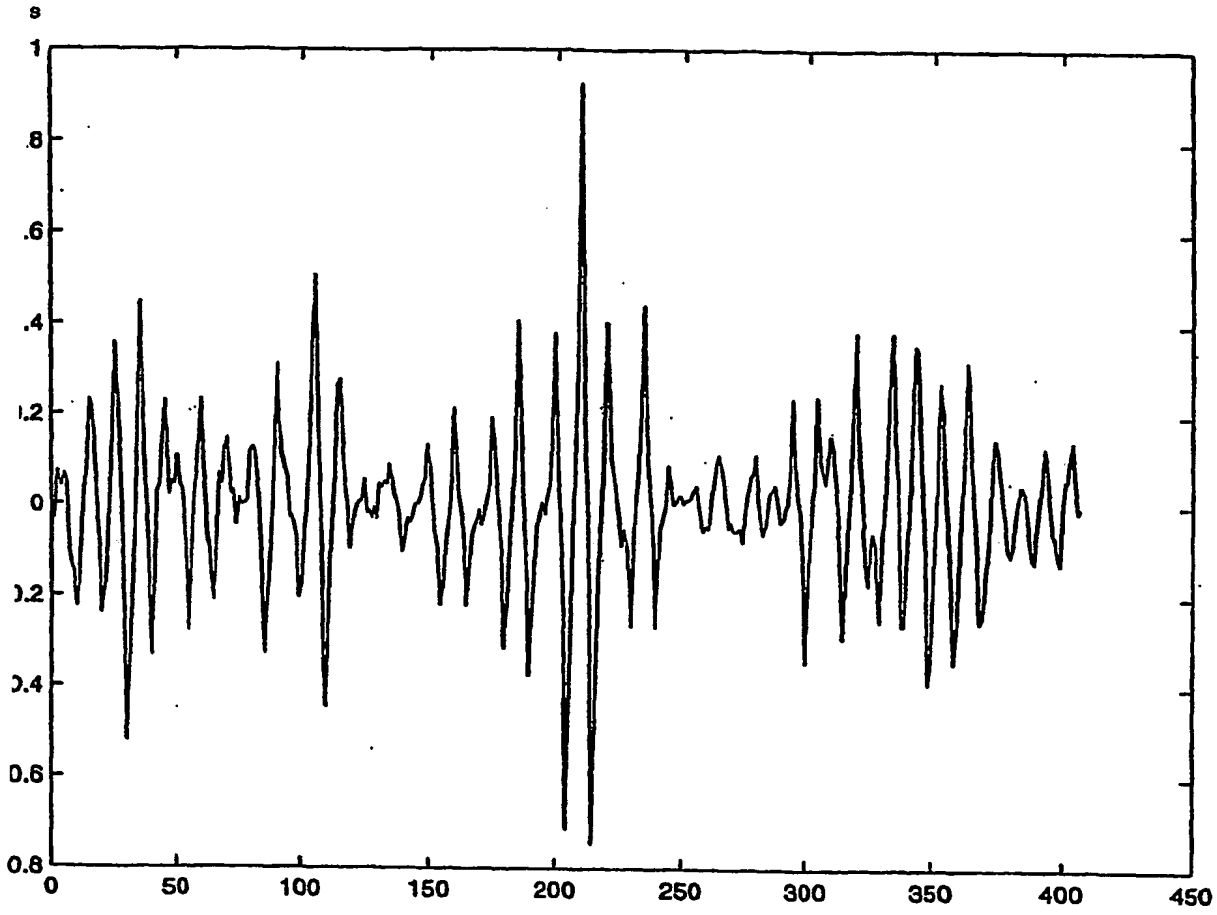


Figure 14

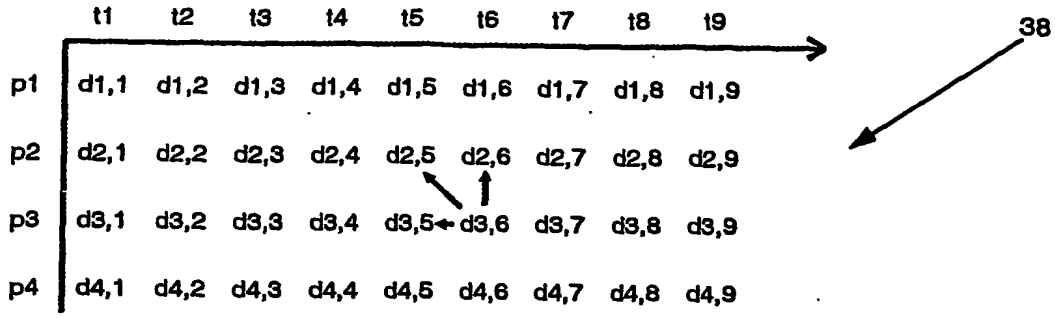

t1 t2 t3 t4 t5 t6 t7 t8 t9
38
p1 d1,1 d1,2 d1,3 d1,4 d1,5 d1,6 d1,7 d1,8 d1,9
p2 d2,1 d2,2 d2,3 d2,4 d2,5 d2,6 d2,7 d2,8 d2,9
p3 d3,1 d3,2 d3,3 d3,4 d3,5 d3,6 d3,7 d3,8 d3,9
p4 d4,1 d4,2 d4,3 d4,4 d4,5 d4,6 d4,7 d4,8 d4,9

Figure 15

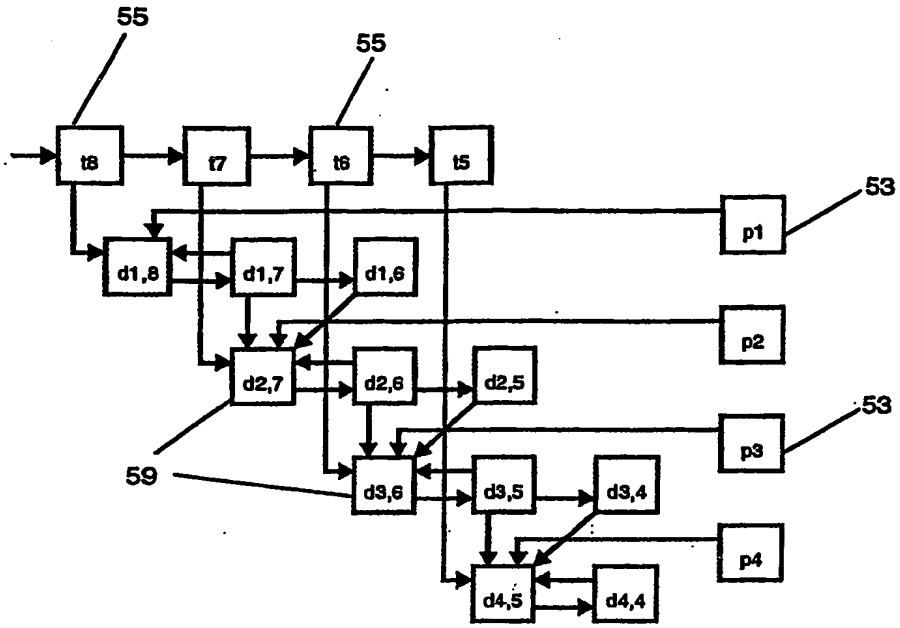

55
55
t8
t7
t6
t5
53
p1
d1,8
d1,7
d1,6
p2
d2,7
d2,6
d2,5
53
p3
59
d3,6
d3,5
d3,4
p4
d4,5
d4,4

Figure 16

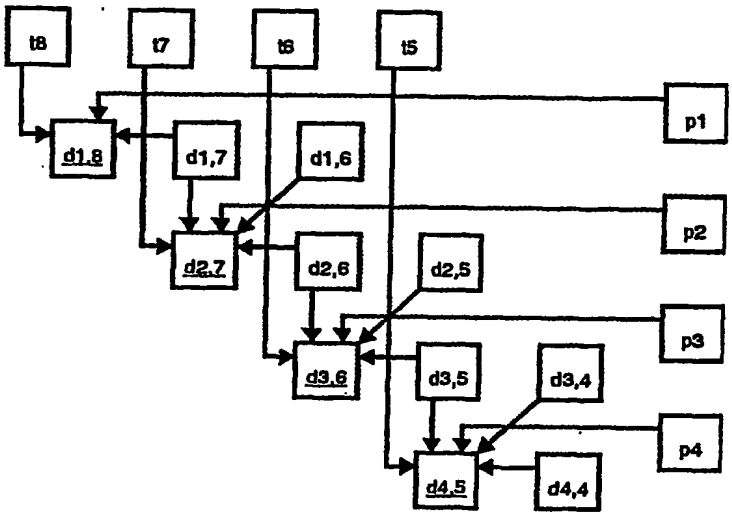
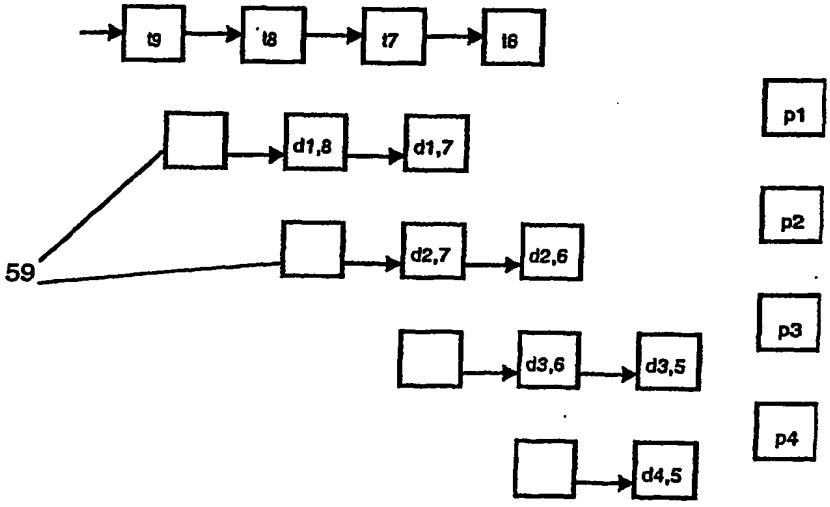

t8
t7
t6
t5
p1
d1,8
d1,7
d1,6
p2
d2,7
d2,6
d2,5
p3
d3,6
d3,5
d3,4
p4
d4,5
d4,4

Figure 17


t9
t8
t7
t6
p1
d1,8
d1,7
p2
59
d2,7
d2,6
p3
d3,6
d3,5
p4
d4,5

	p	q	r	a	x	a	b	c	s	t	v	q	...
a	-1	-1	-1	2	1	2	1	0	-1	-1	-1	-1	
x	-1	-2	-2	1	4	3	2	1	0	-1	-2	-2	
b	-1	-2	-3	0	3	2	5	4	3	2	1	0	
a	-1	-2	-3	-1	2	1	4	3	2	1	0	-1	
c	-1	-2	-3	-2	1	0	3	6	5	4	3	2	
s	-1	-2	-3	-3	0	-1	2	5	8	7	6	5	

Figure 19

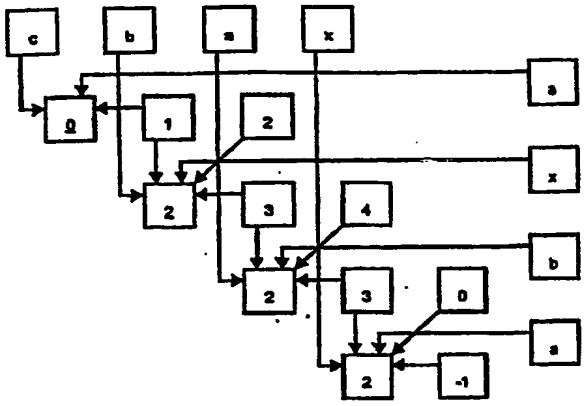


Figure 20

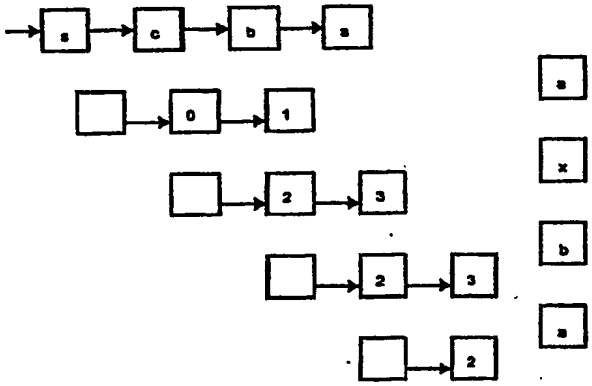


Figure 21

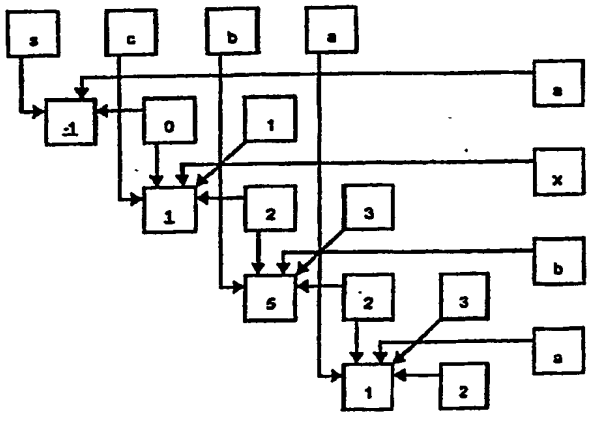


Figure 22

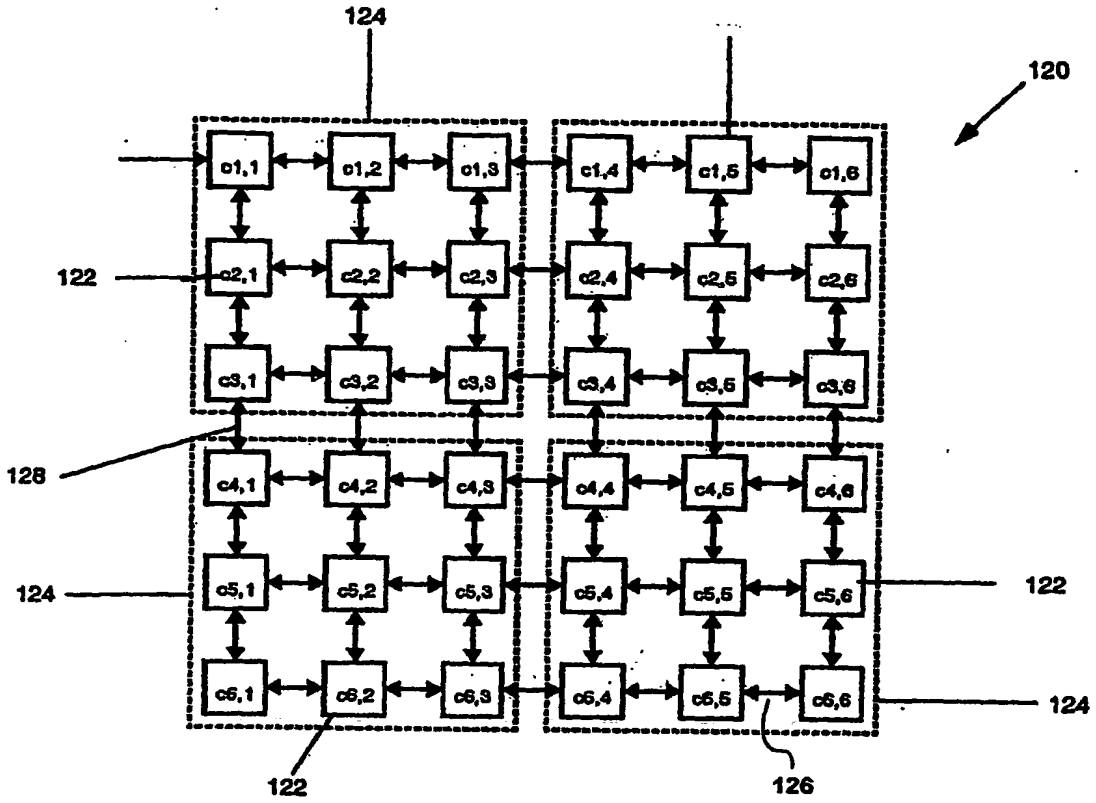

124
120
122
128
124
122
122
126
124
c1,1
c1,2
c1,3
c1,4
c1,5
c1,6
c2,1
c2,2
c2,3
c2,4
c2,5
c2,6
c3,1
c3,2
c3,3
c3,4
c3,5
c3,6
c4,1
c4,2
c4,3
c4,4
c4,5
c4,6
c5,1
c5,2
c5,3
c5,4
c5,5
c5,6
c6,1
c6,2
c6,3
c6,4
c6,5
c6,6

Figure 23

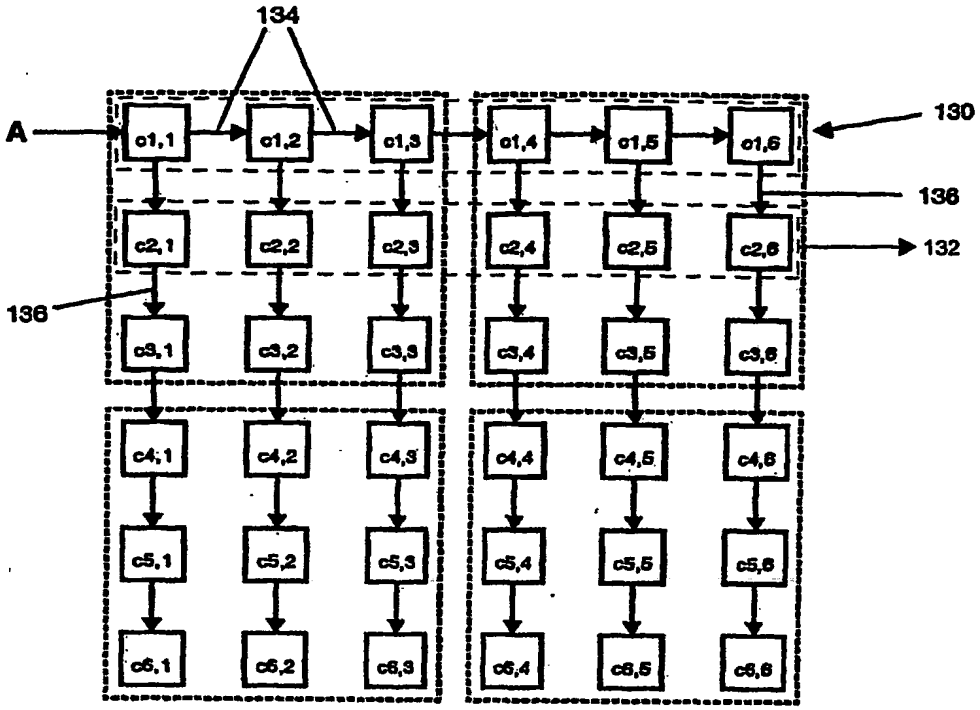

134
A
c1,1
c1,2
c1,3
c1,4
c1,5
c1,6
130
136
c2,1
c2,2
c2,3
c2,4
c2,5
c2,6
132
136
c3,1
c3,2
c3,3
c3,4
c3,5
c3,6
c4,1
c4,2
c4,3
c4,4
c4,5
c4,6
c5,1
c5,2
c5,3
c5,4
c5,5
c5,6
c6,1
c6,2
c6,3
c6,4
c6,5
c6,6

Figure 24

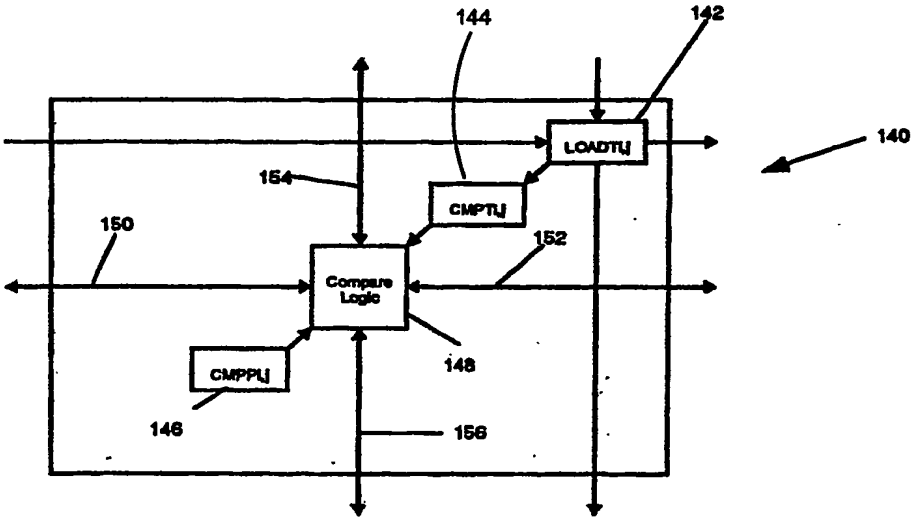

144
142
140
LOADTU
154
CMPTU
150
152
Compare Logic
148
CMPPU
146
156

Figure 25

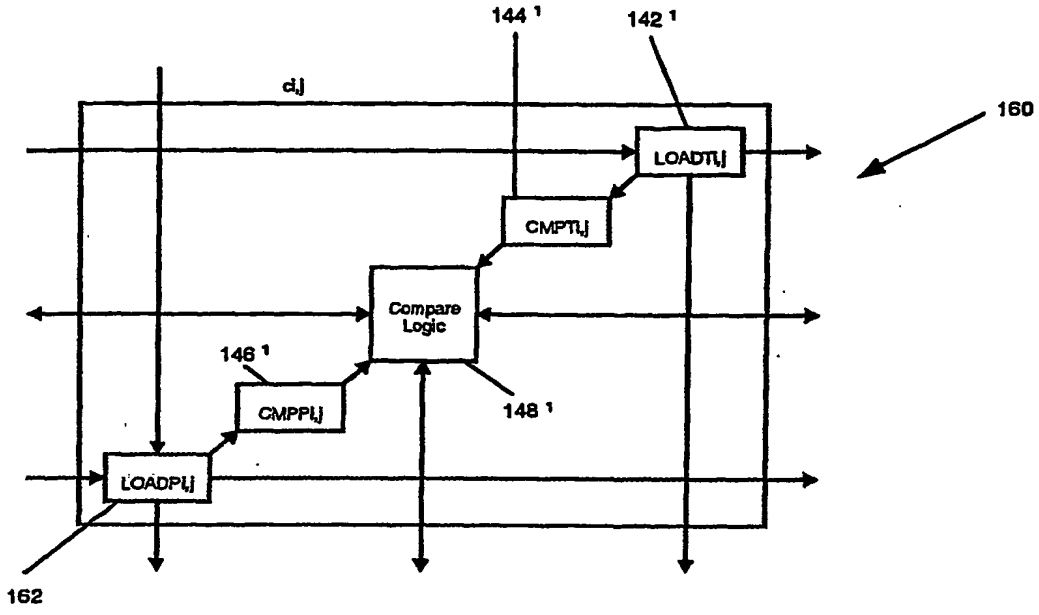

144 1
142 1
c,j
160
LOADTi,j
CMPTi,j
Compare Logic
146 1
CMPPi,j
148 1
LOADPi,j
162

Figure 26

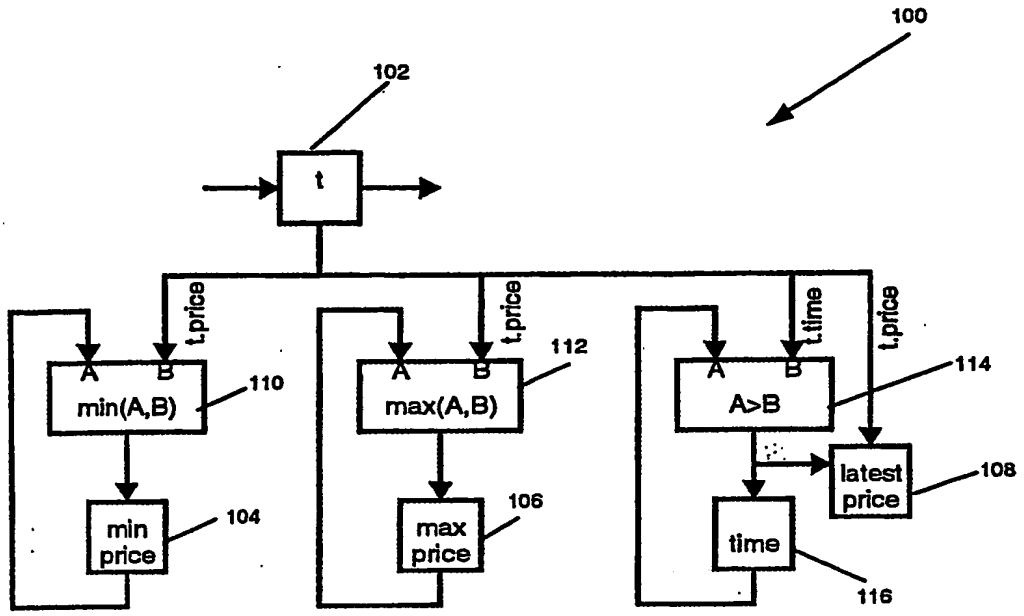

100
102
t
t.price
t.price
t.time
t.price
A
B
min(A,B)
110
min price
104
A
B
max(A,B)
112
max price
106
A
B
A>B
114
latest price
108
time
116

Figure 27

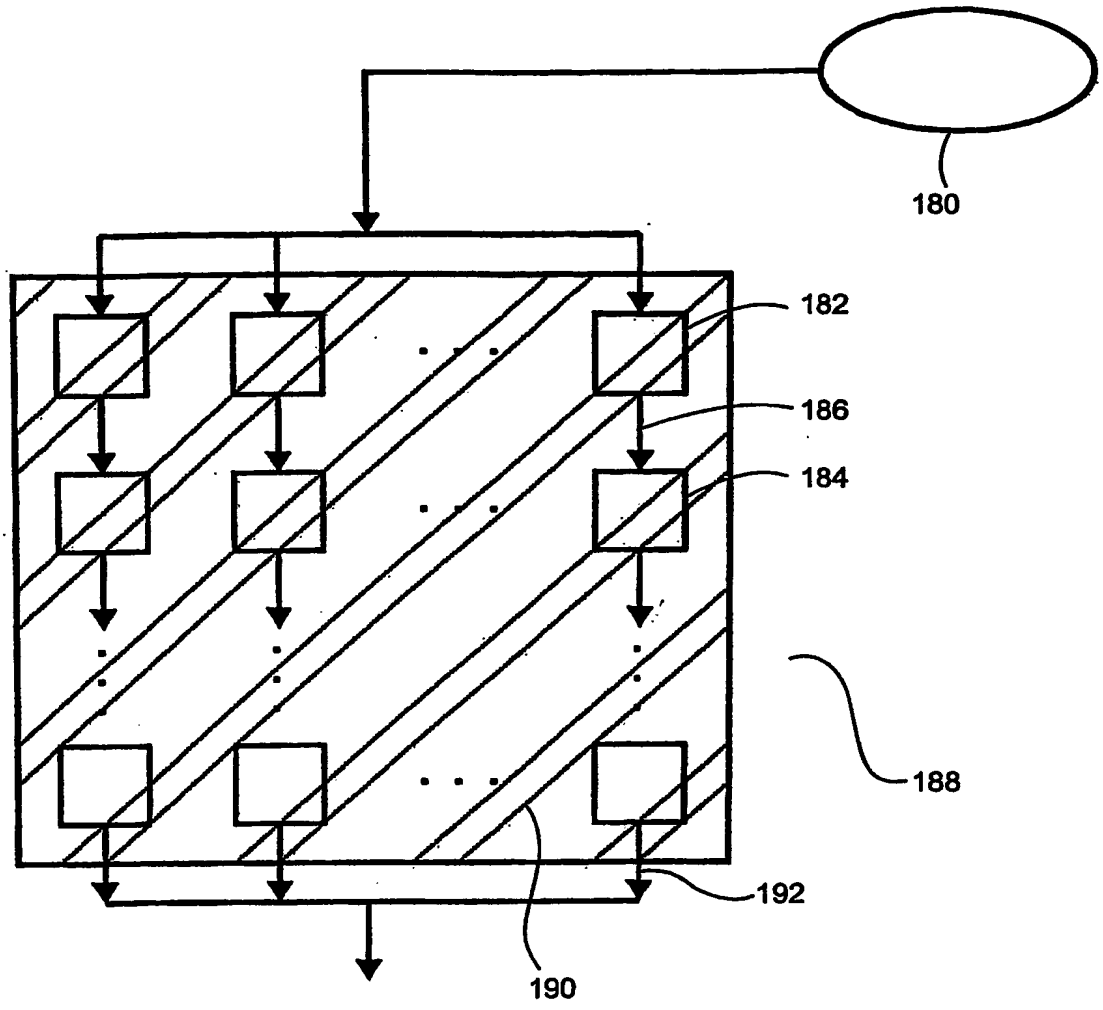


Fig. 28

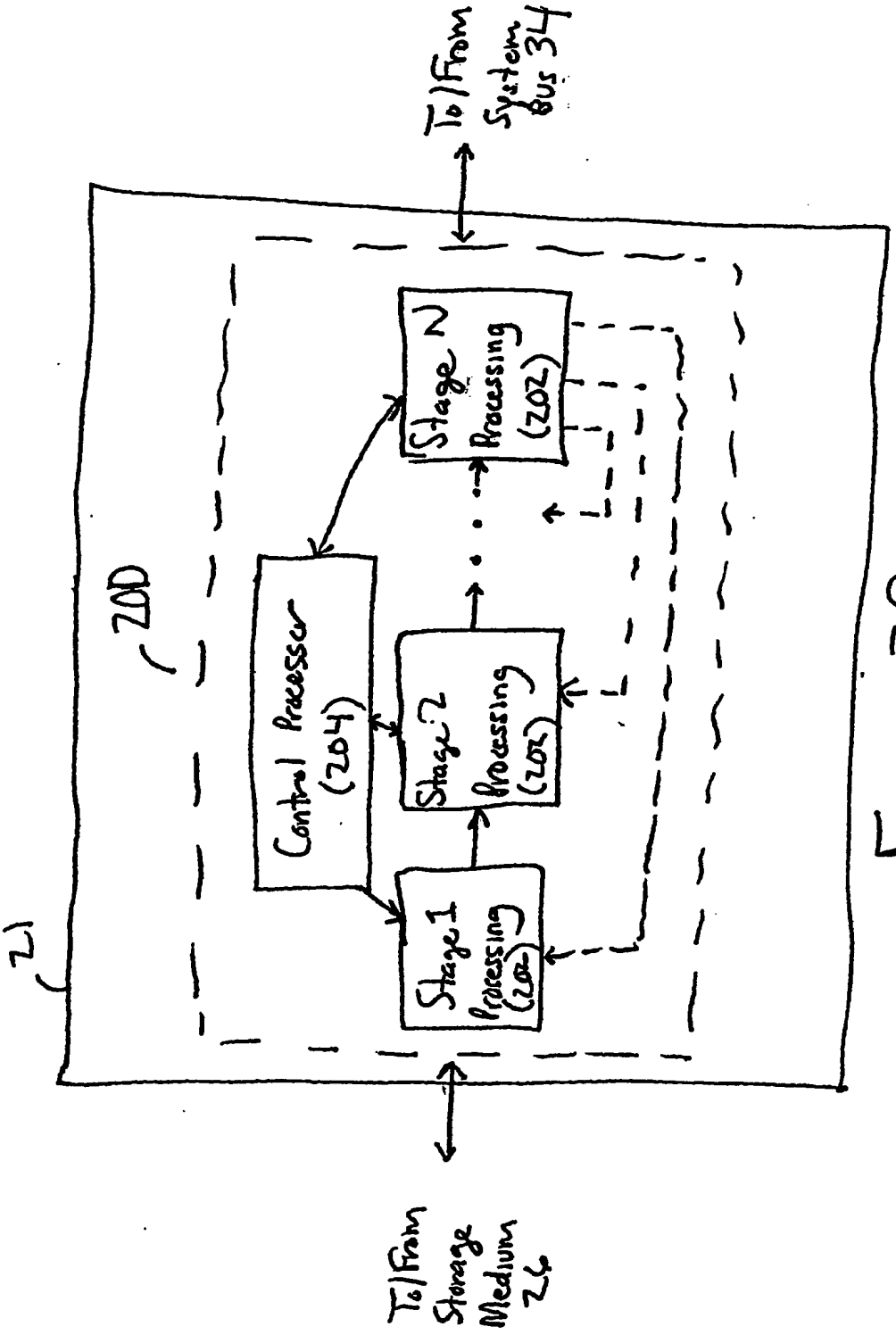

To/From System Bus 34
200
Control Processor (204)
Stage 1 Processing (206)
Stage 2 Processing (208)
Stage N Processing (202)
To/From Storage Medium 26

Figure 29

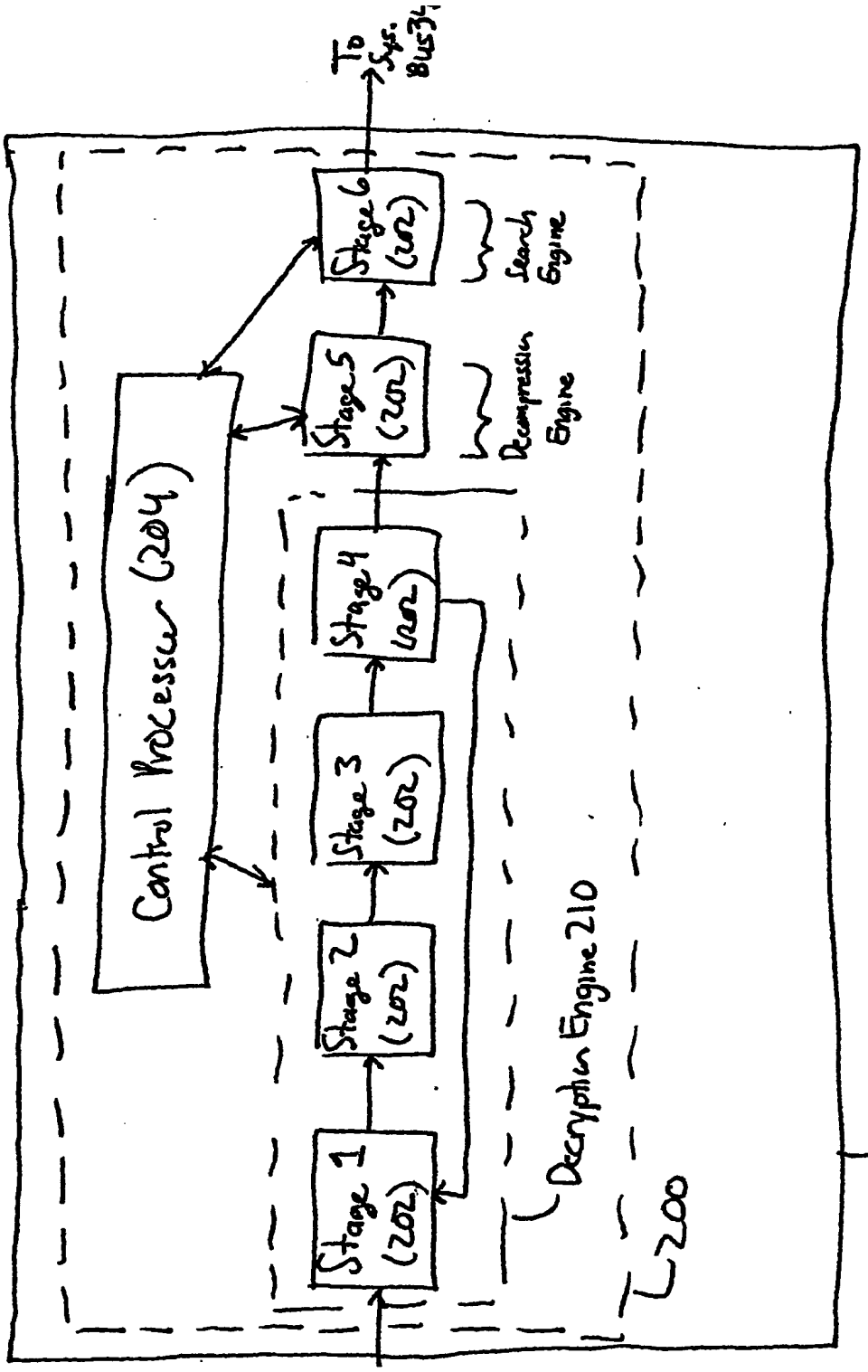

To Sys. Bus 34
Stage 6 (202)
Search Engine
Stage 5 (202)
Decompression Engine
Stage 4 (202)
Stage 3 (202)
Stage 2 (202)
Stage 1 (202)
Control Processor (204)
Decryption Engine 210
200
21

Figure 30

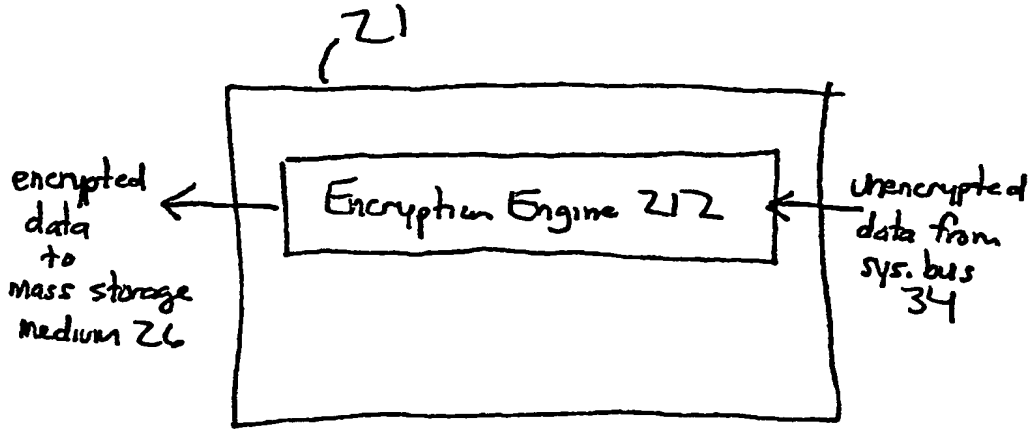


Figure 31

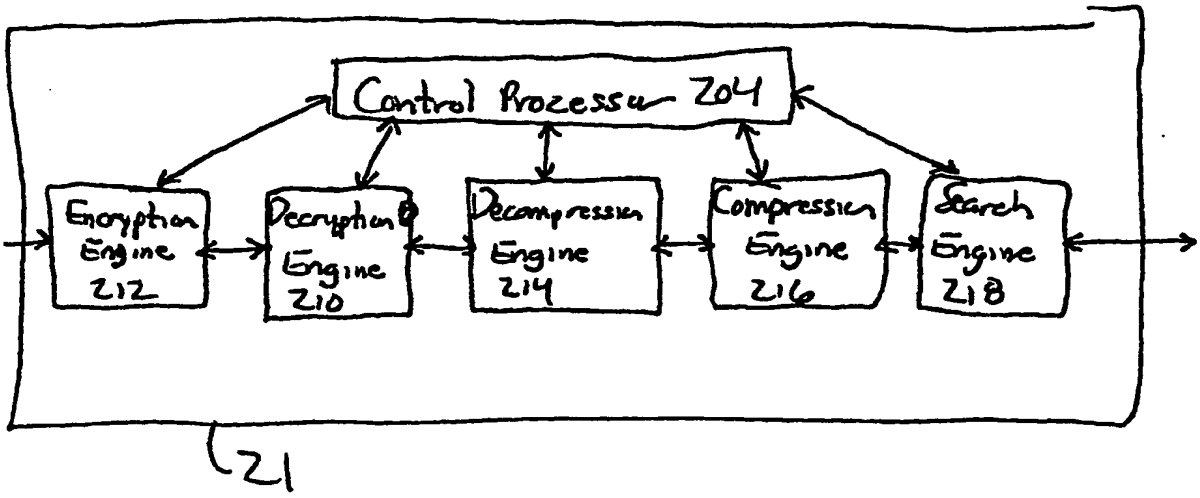
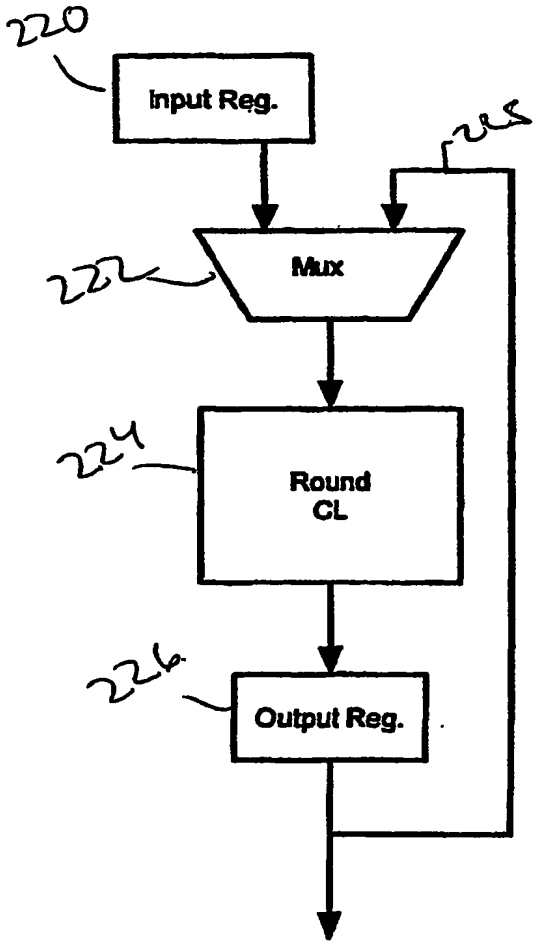
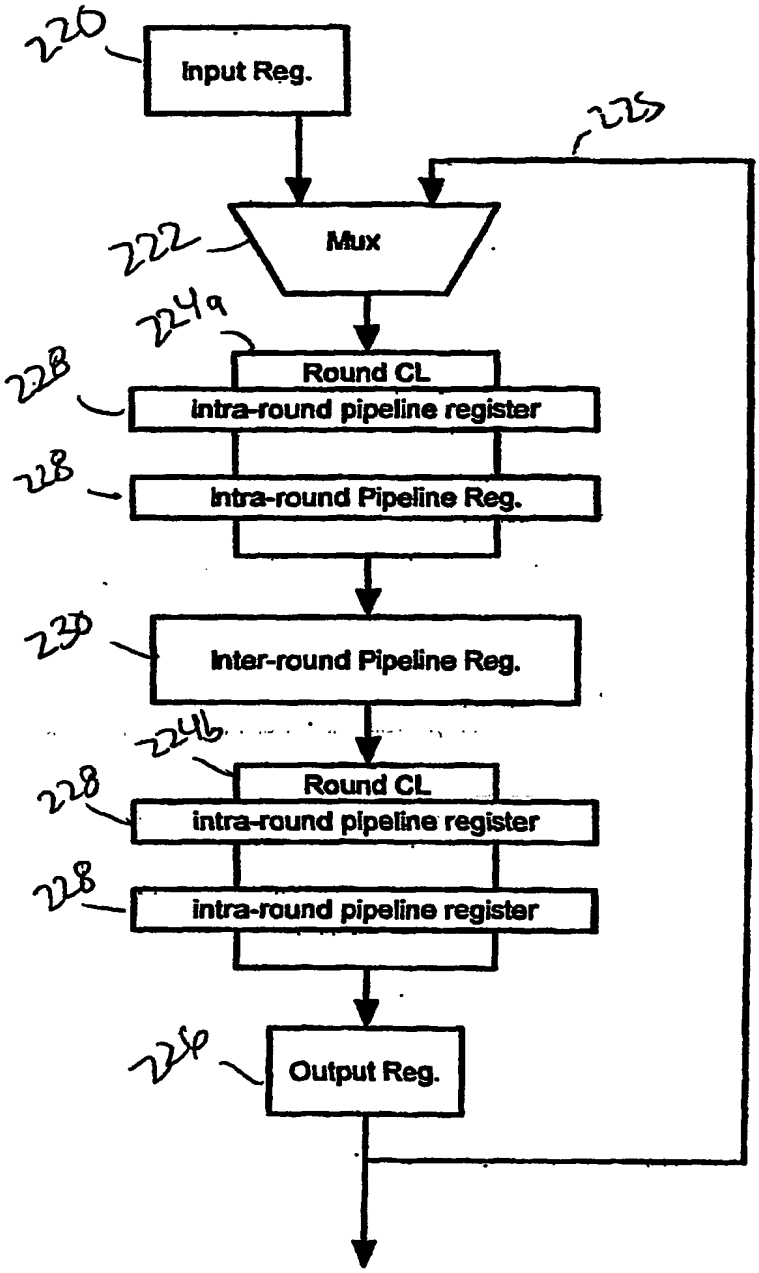


Figure 32



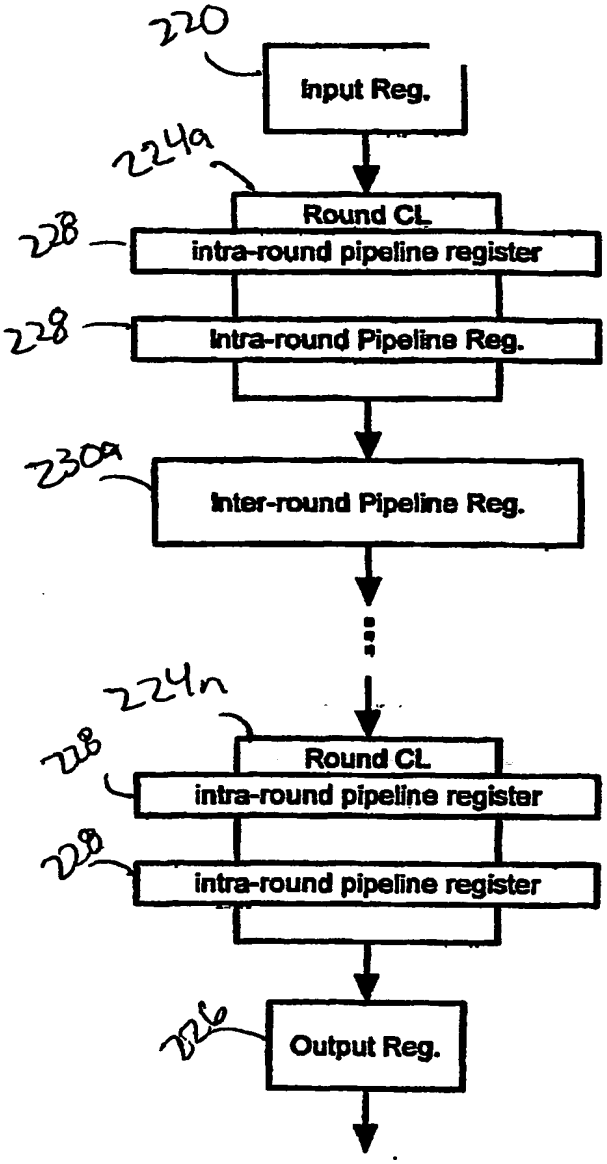
Single stage encryption/decryption engine.

Figure 33



Pipelined encryption/decryption engine.

Figure 34



Fully pipelined encryption/decryption engine.

Figure 35

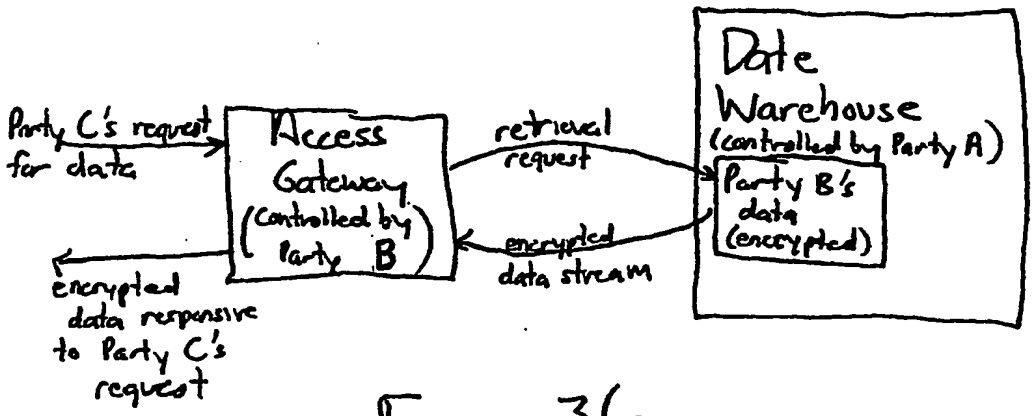

Party C's request for data
Access Gateway (Controlled by Party B)
retrieval request
encrypted data stream
Date Warehouse (controlled by Party A)
Party B's data (encrypted)
encrypted data responsive to Party C's request

Figure 36

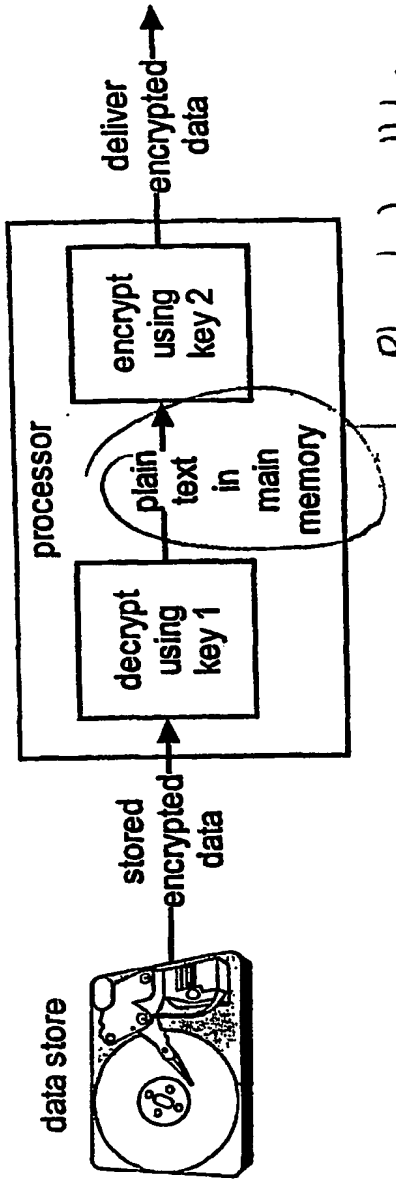

data store
stored encrypted data
processor
decrypt using key 1
plain text in main memory
encrypt using key 2
deliver encrypted data
Plan text will be accessible by malware if processor is compromi

Figure 37

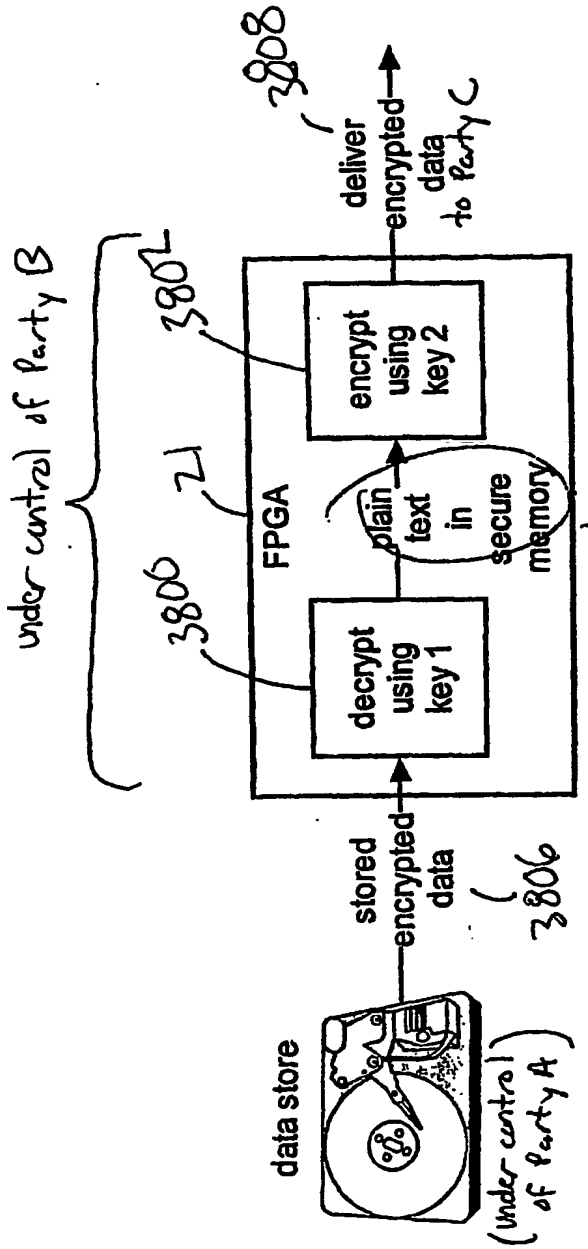

under control of Party B
3808
deliver encrypted data to Party C
3802
encrypt using key2
21
FPGA
plain text in secure memory
3806
decrypt using key1
stored encrypted data
3806
data store
(under control of Party A)
Plain text is inaccessible to a remote processor that is compromised by malware

Figure 38

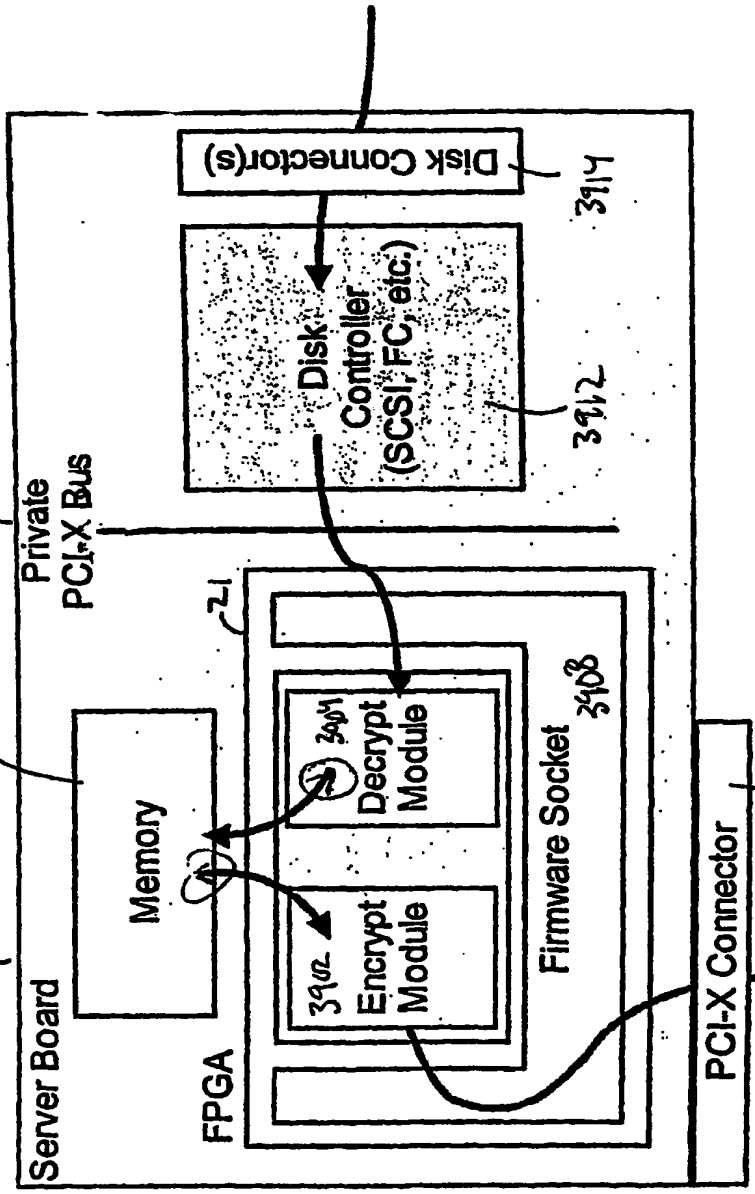

Server Board
3600
Memory
3906
FPGA
Private PCI-X Bus
3910
Disk Controller (SCSI, FC, etc.)
3912
Disk Connector(s)
3914
Decrypt Module
3904
Encrypt Module
3902
Firmware Socket
3908
PCI-X Connector
3916
To Comp. Mem. Interface
34

Figure 39(a)

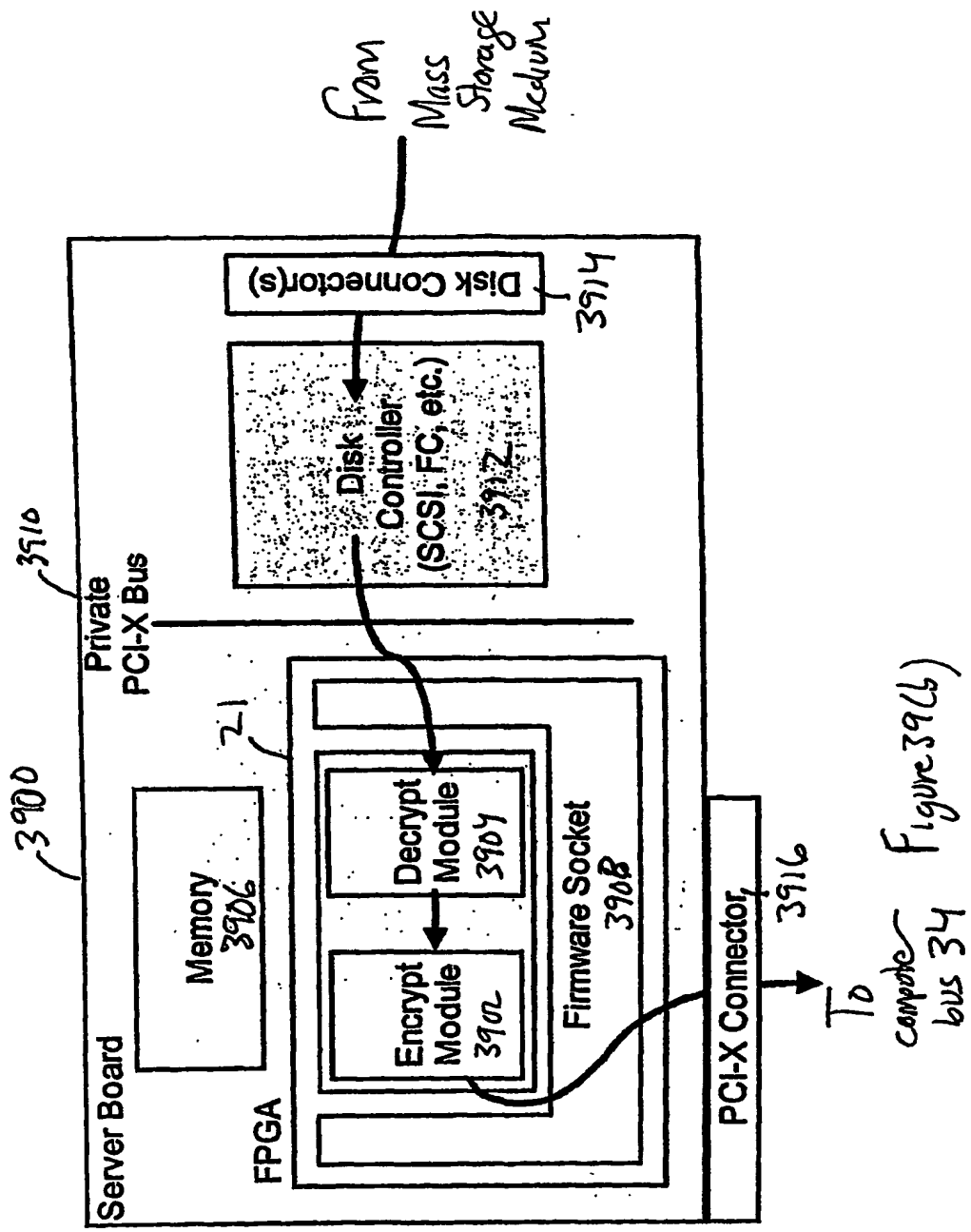

From Mass Storage Medium
Disk Connector(s)
3914
Disk Controller (SCSI, FC, etc.)
3912
3910
Private PCI-X Bus
3900
Server Board
Memory 3906
FPGA
Decrypt Module 3904
Encrypt Module 3902
Firmware Socket 3908
PCI-X Connector
3916
To compute bus 34

Figure 39(b)

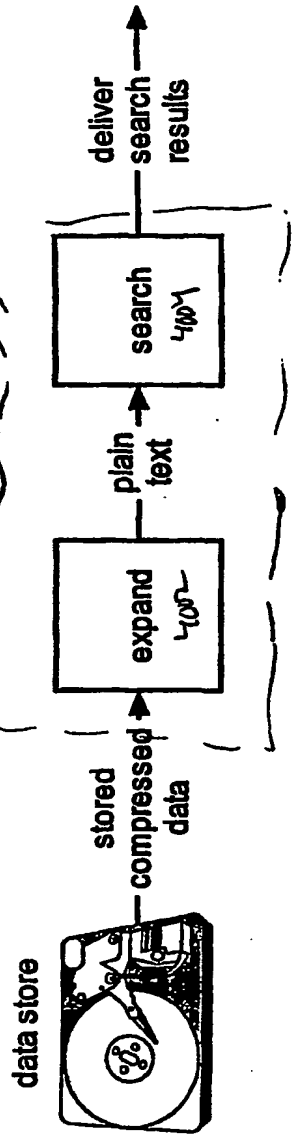

data store
stored compressed data
expand
plain text
search
deliver search results
21

Figure 40

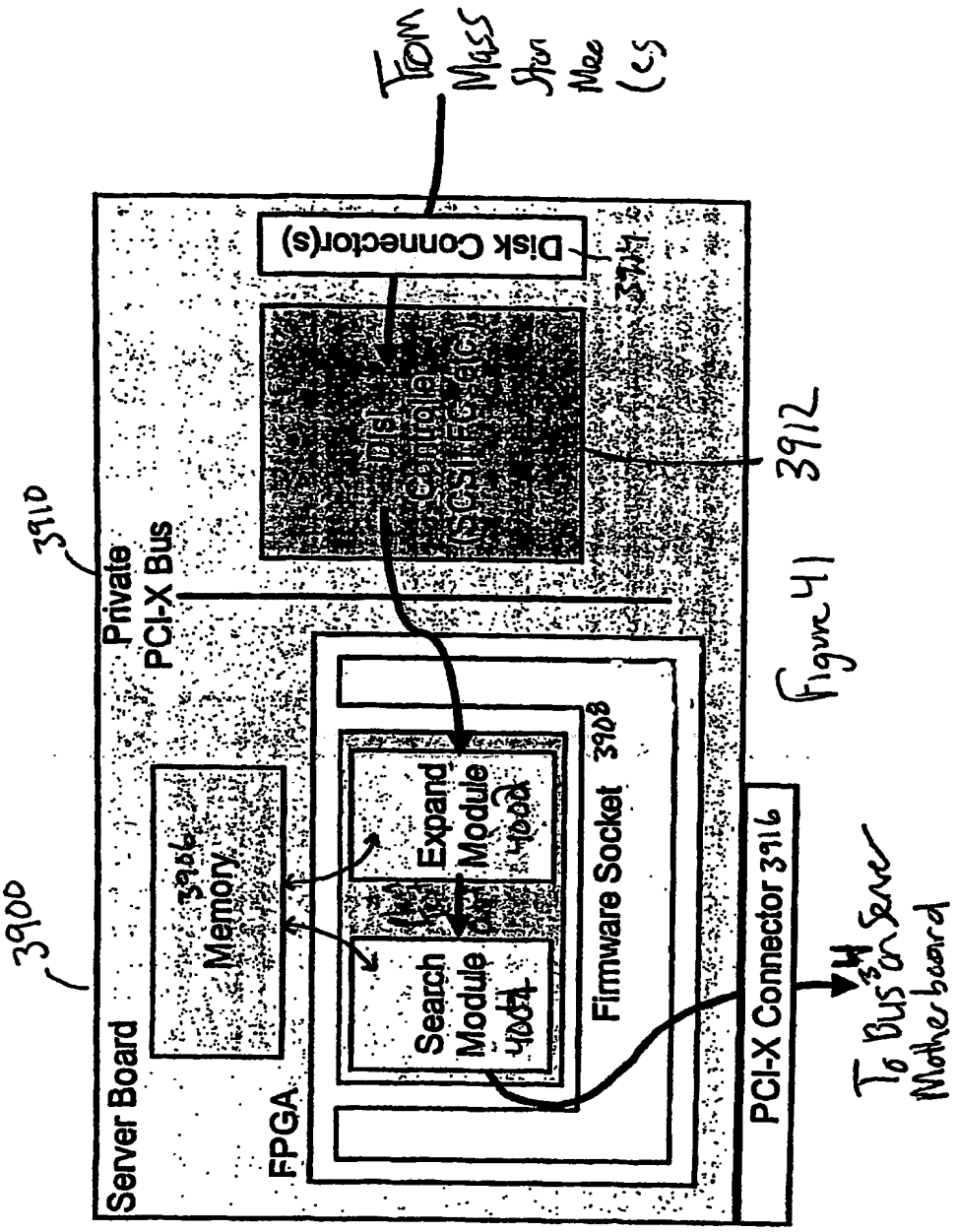

From Mass Storage Device(s)
Disk Connector(s)
3914
3912
3910
Private PCI-X Bus
3900
Server Board
3906
Memory
FPGA
Search Module 4004
Expand Module 4002
Firmware Socket 3908
PCI-X Connector 3916
To Bus on Server Motherboard

Figure 41

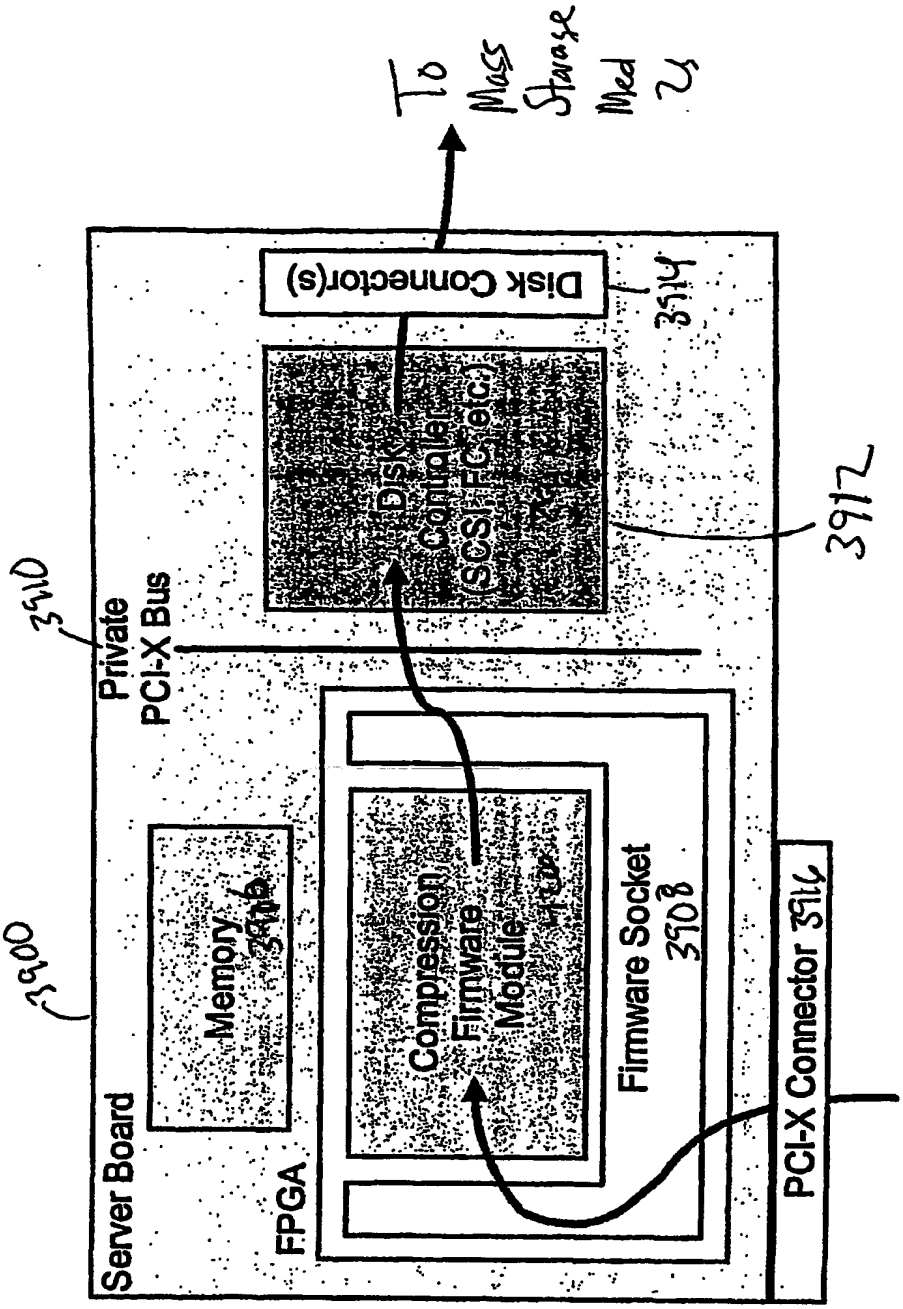

To Mass Storage Med 24
Disk Connector(s)
3914
Disk Controller (SCSI, FC, etc.)
3912
3910
Private PCI-X Bus
3900
Server Board
Memory 3906
FPGA
Compression Firmware Module
Firmware Socket 3908
PCI-X Connector 3916
From system bus 34

Figure 42

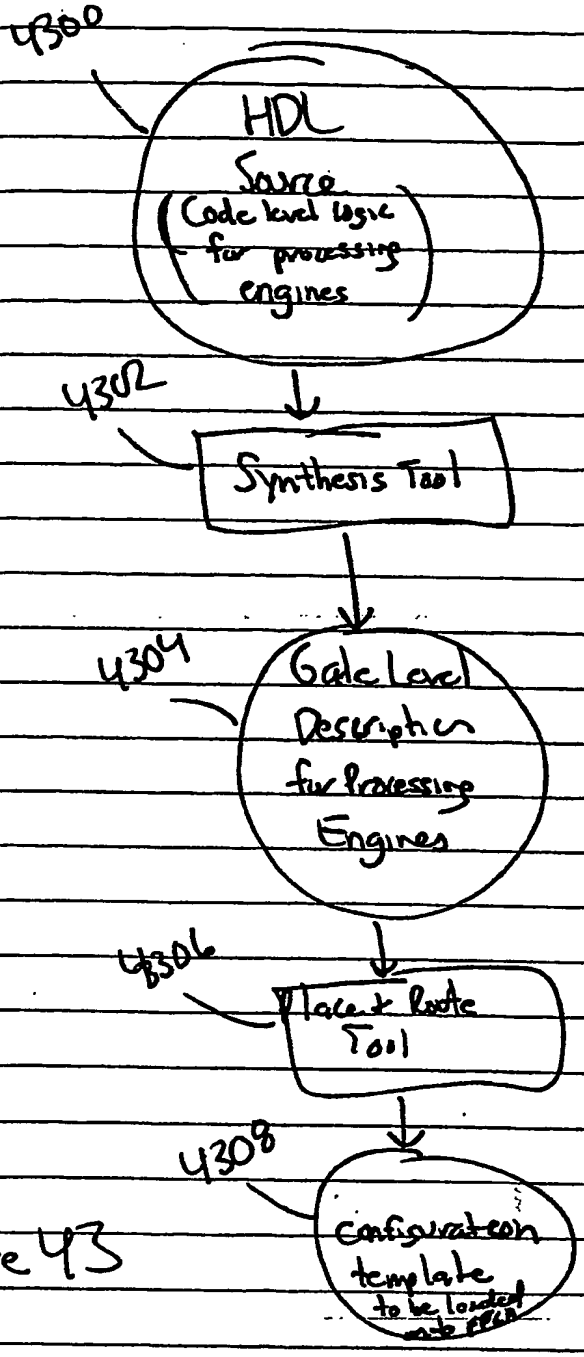
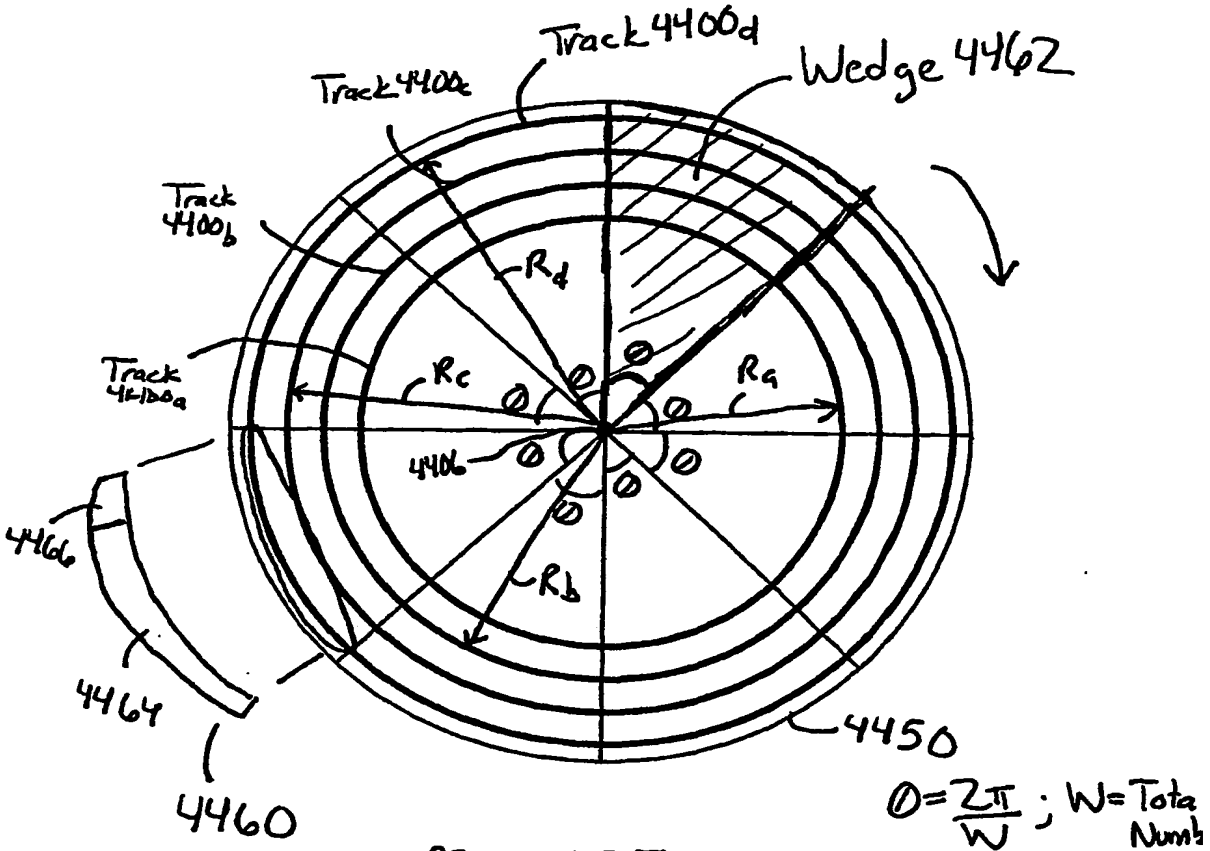

4300
HDL Source
(Code level logic for processing engines)
4302
Synthesis Tool
4304
Gate Level Description for Processing Engines
4306
Place & Route Tool
4308
Configuration template to be loaded into FPGA

Figure 43



PRIOR ART

Figure 44(a)

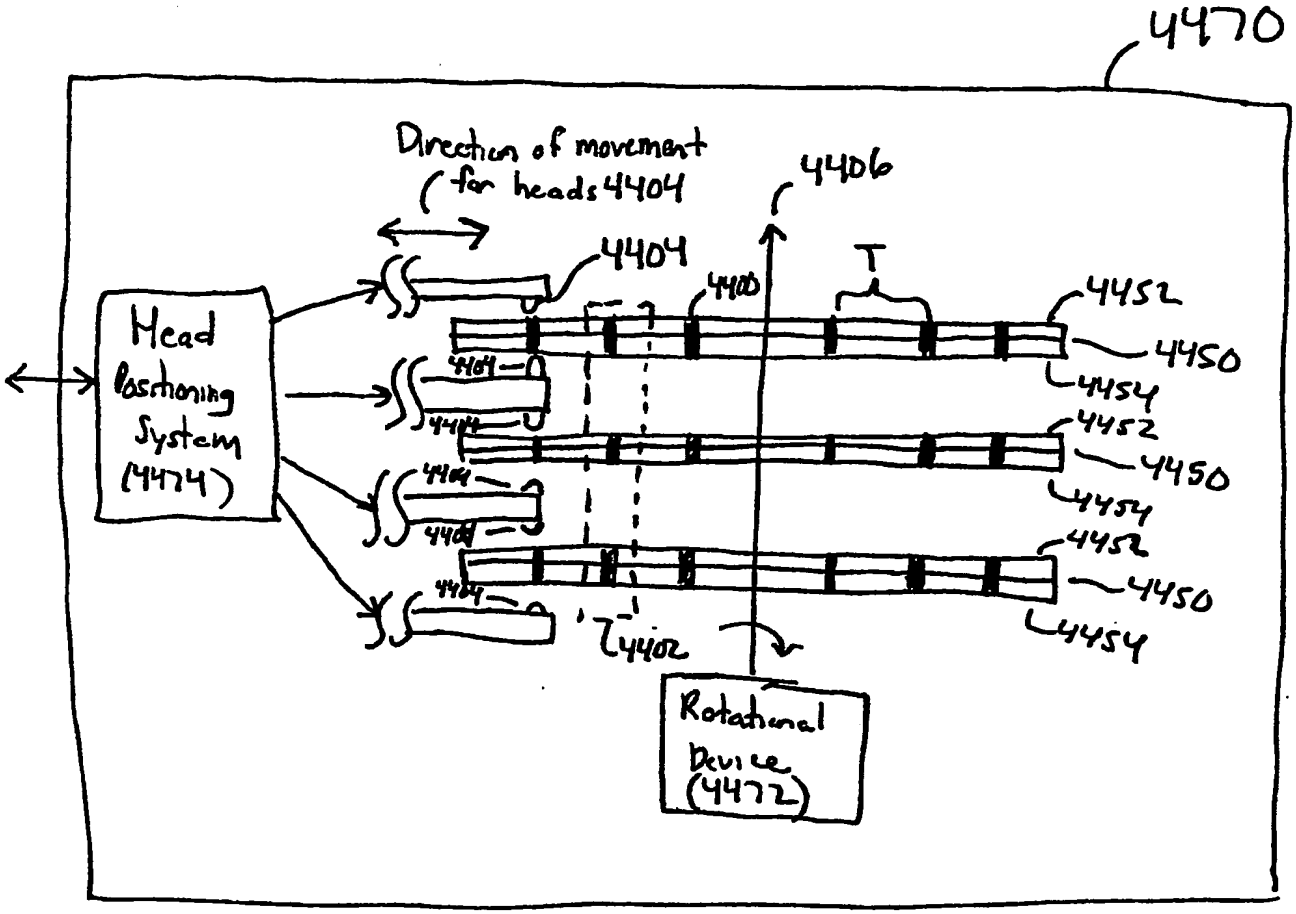

4470
Direction of movement (for heads 4404)
4406
4404
T
4452
4450
4454
Head Positioning System (4474)
4402
Rotational Device (4472)

Figure 44(b)

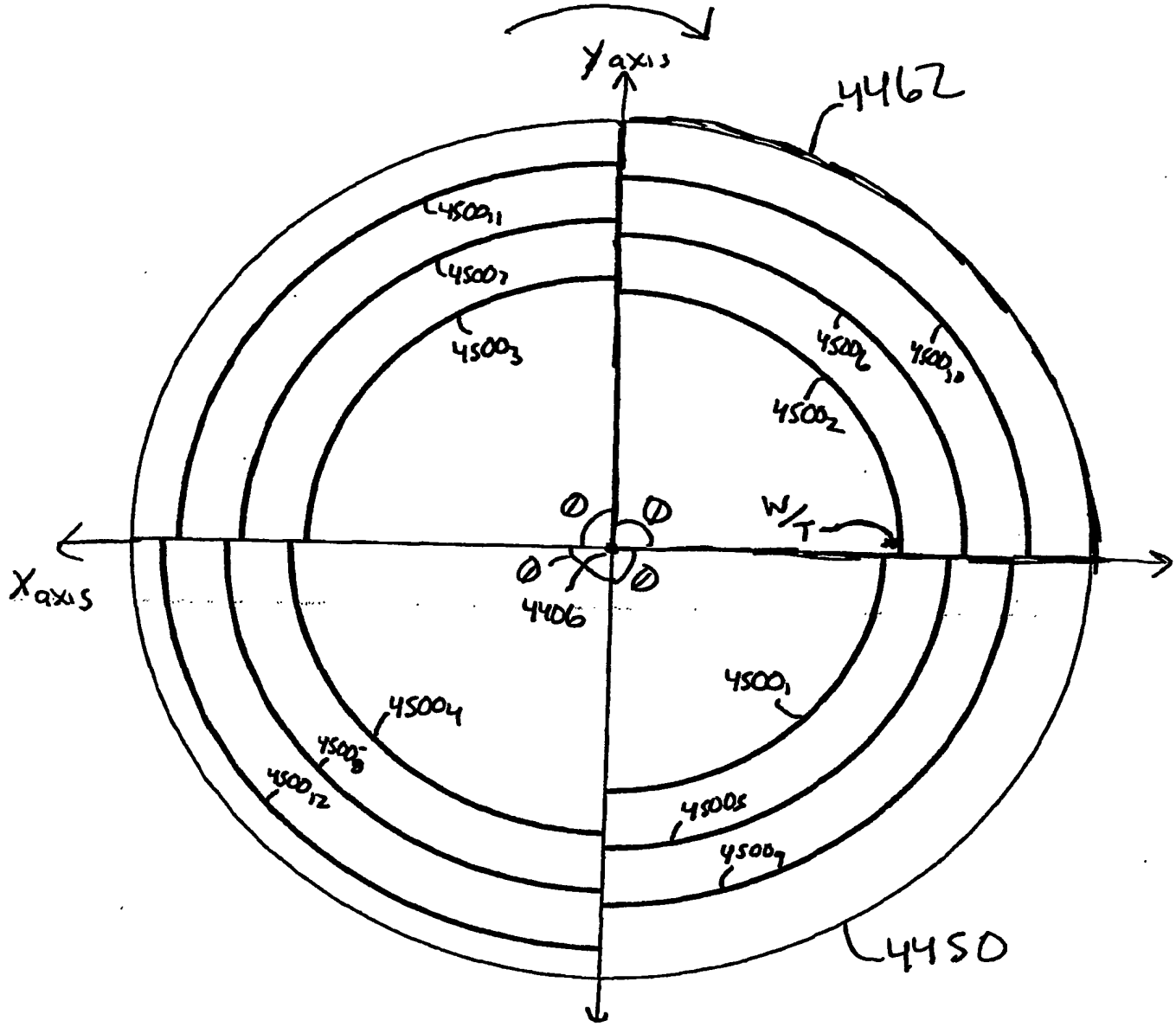

Y axis
4462
4500 11
4500 7
4500 3
4500 6
4500 10
4500 2
W/T
X axis
4406
4500 1
4500 4
4500 8
4500 12
4500 5
4500 9
4450

Figure 45

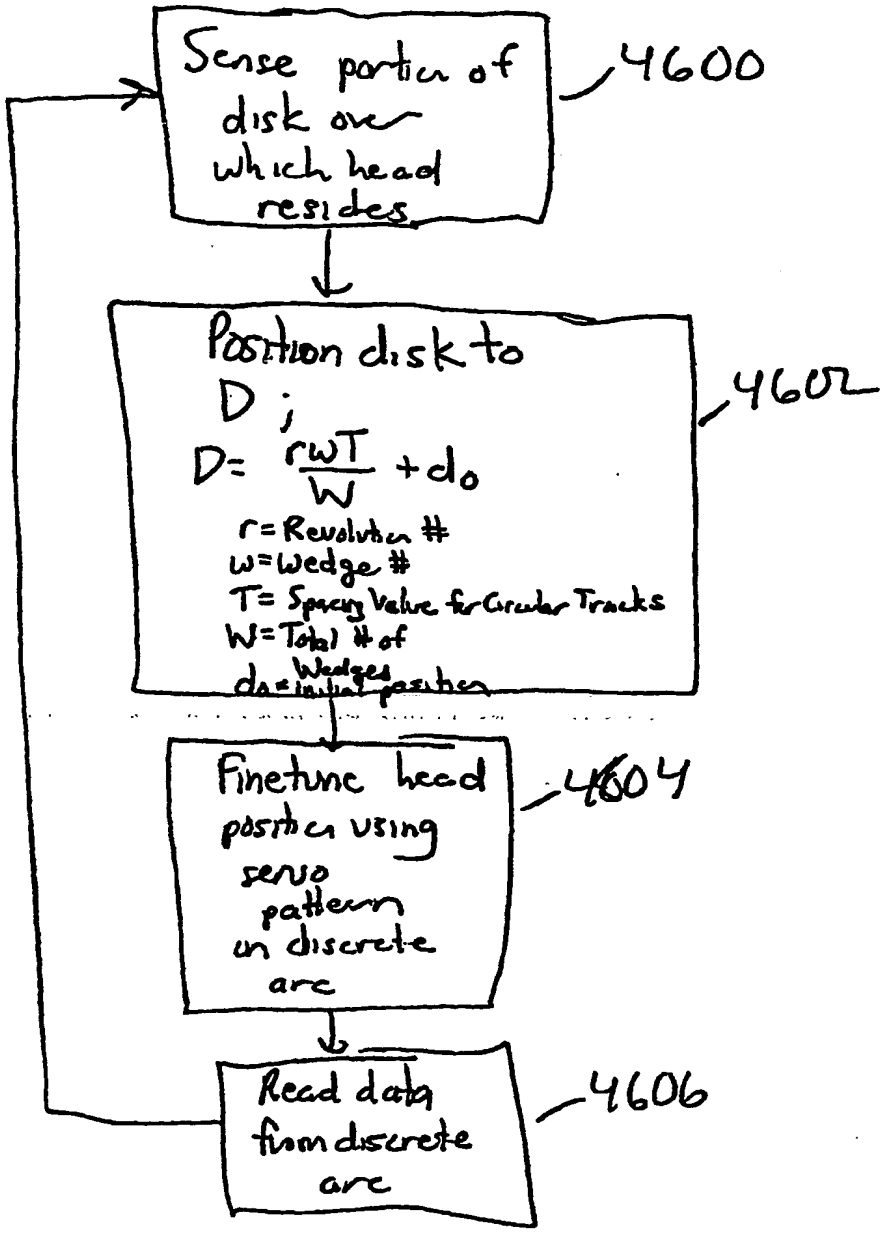

Sense portion of disk over which head resides
4600
Position disk to D;
$D = \frac{rwT}{W} + d_0$
r = Revolution #
w = Wedge #
T = Spacing Value for Circular Tracks
W = Total # of Wedges
d_0 = Initial position
4602
Finetune head position using servo pattern on discrete arc
4604
Read data from discrete arc
4606

Figure 46

Figure 47(a)

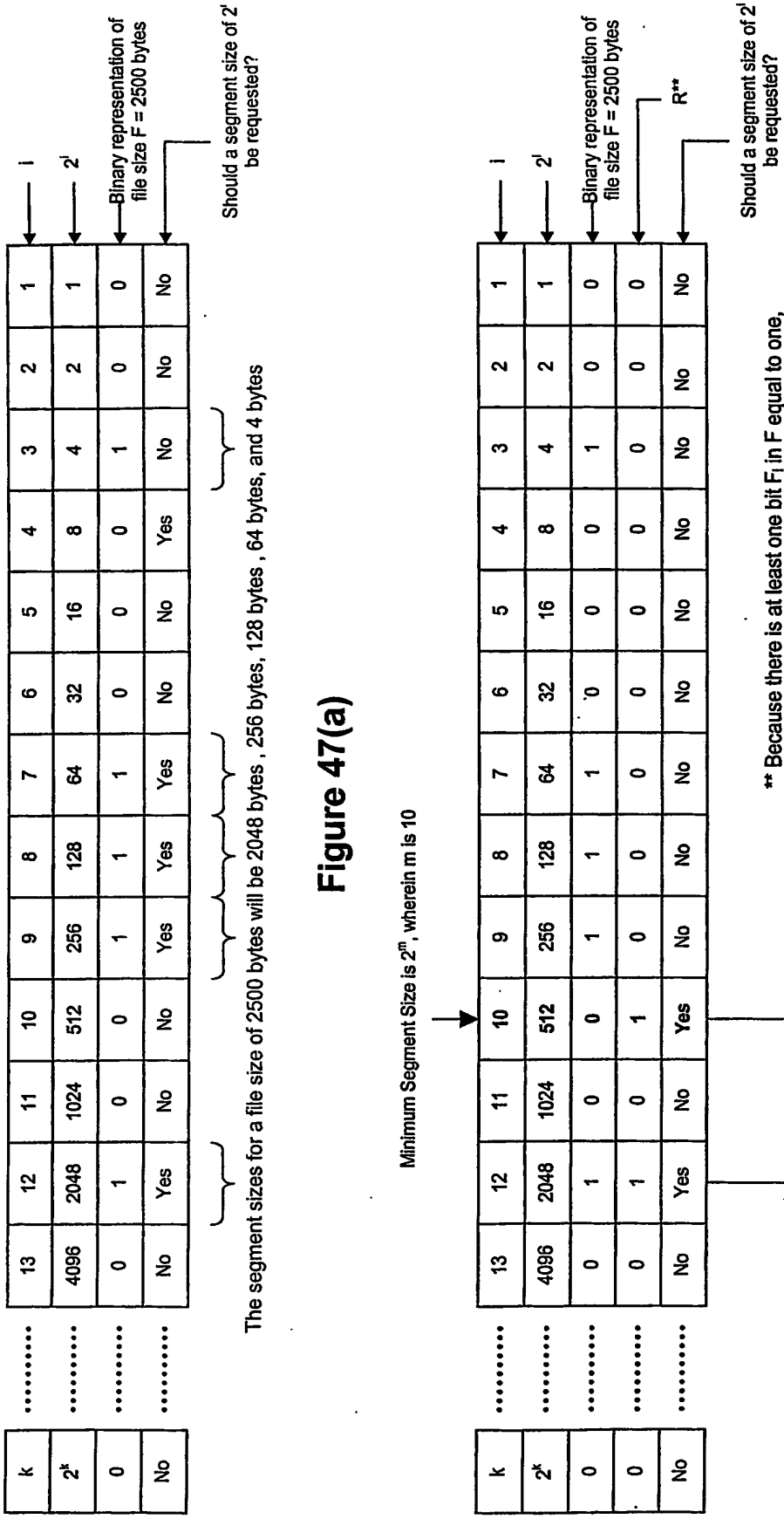


Figure 47(b)

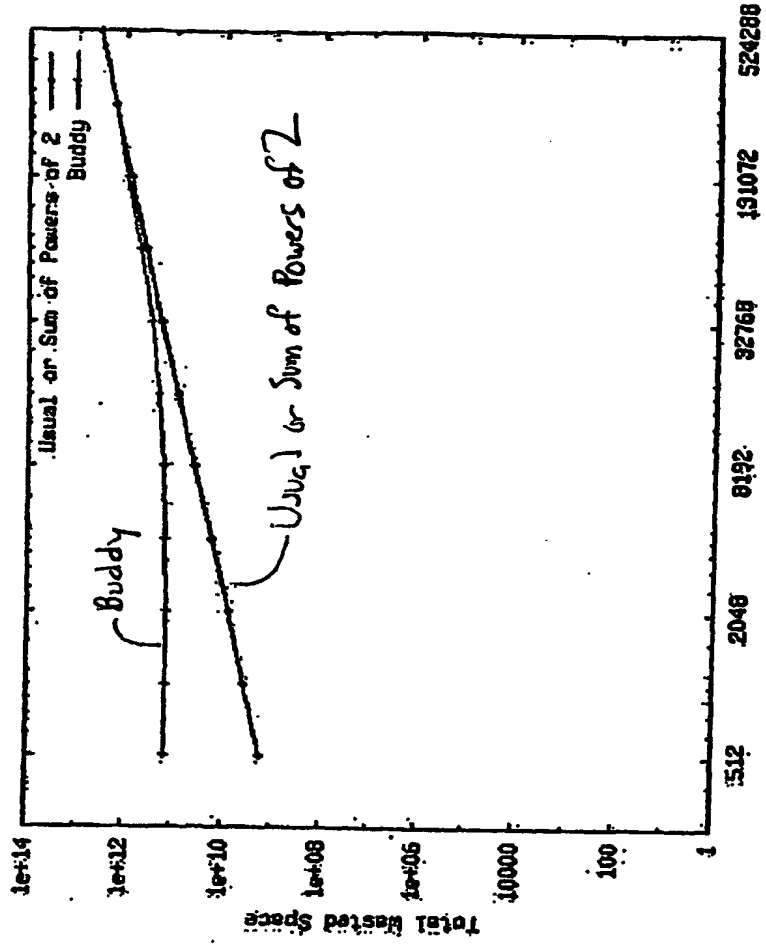

Usual or Sum of Powers of 2
Buddy
Buddy
Usual or Sum of Powers of 2
Total Wasted Space
1e+14
1e+12
1e+10
1e+08
1e+06
10000
100
1
512
2048
8192
32768
131072
524288
Minimum Segment Size
Wasted storage due to internal fragmentation.

Figure 48

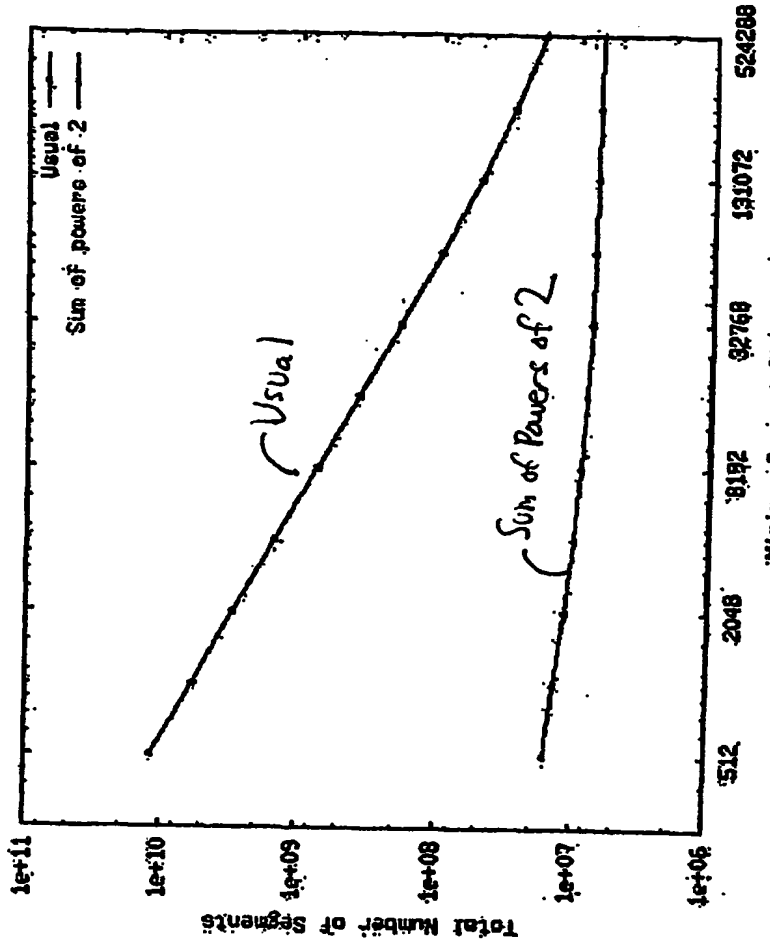

Usual
Sum of powers of 2
Usual
Sum of Powers of 2
Total Number of Segments
1e+11
1e+10
1e+09
1e+08
1e+07
1e+06
512
2048
8192
32768
131072
524288
Minimum Segment Size
Total number of segments in the file system.

Figure 49

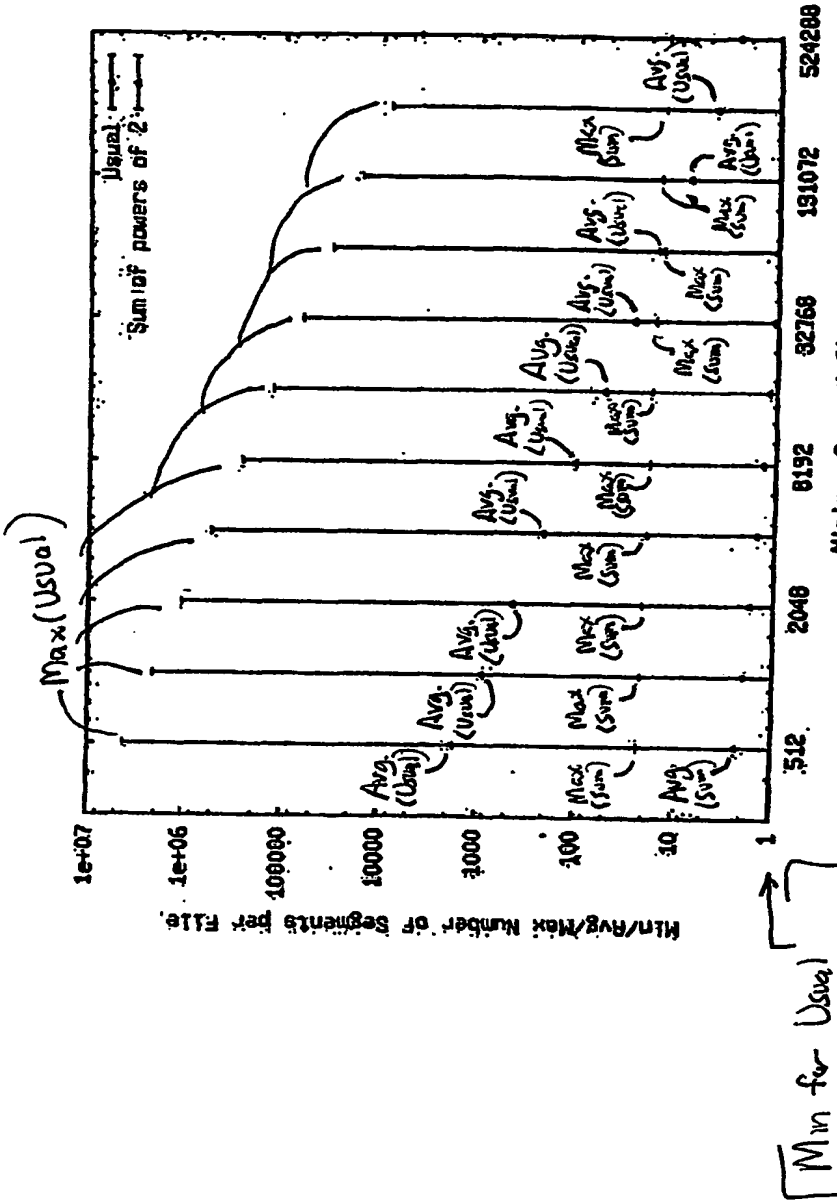

Max(Usual)
Usual
Sum of powers of 2
Min/Avg/Max Number of Segments per File.
1e+07
1e+06
100000
10000
1000
100
10
1
512
2048
8192
32768
131072
524288
Minimum Segment Size
Number of segments per file.
Min for Usual and Sum of Powers of 2 is 1

Figure 5D

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